Ninth Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

Douglas Kim, Rohith Ramachandran, Nageswara R Gunupudi, Kostas Kokkinakis, Vani Gopalakrishna, Nasser Kehtarnavaz, Murat Torlak, , Lakshmish Ramanna, Arthur Lobo and Philipos C. Loizou

Department of Electrical Engineering
University of Texas-Dallas
Richardson, TX 75080
Email: loizou@utdallas.edu

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Work in this quarter focused on completing the testing of the SDIO interface board (v.2). We successfully tested the SDIO interface board and demonstrated that it is capable of capturing binaural inputs from two microphones (one in each ear) and processing these two signals via the ACE algorithm in real-time. We started designing the final SDIO interface board incorporating the following changes in the revision: (1) reduction in board size by eliminating unnecessary components or choosing smaller parts and (2) provision for an enclosure (packaging) of the board. We also finished a real-time implementation of the beamforming algorithm, which is suitable for researchers interested in bilateral implant studies. Finally, we report on steps taken to further optimize the implementation of the ACE algorithm by evaluating a recursive approach to compute the Fast Fourier Transform (FFT).

2.1 Final revision of SDIO interface board

We successfully debugged and tested the SDIO interface board (v.2). We are able to run the ACE algorithm in real-time with bilateral inputs (see setup in Figure 1). As shown in Figure 1, the board allows for the acquisition of binaural inputs from the two microphones (one in each ear) embedded in the BTEs (Figure 1). It can therefore be used for unilateral and bilateral cochlear implant users.

We are now moving toward making the final revision of the board. The primary change in design for this revision is the reduction in board size. The secondary change in design will be the provision of appropriate changes to the board layout to accommodate for packaging (enclosure). In order to reduce the overall size of the board, we considered making several small changes to the board such as substituting relatively large existing parts for smaller parts. Other changes included replacing all through-hole test points with miniature test points and removing unnecessary jumpers or other components that are no longer needed. We will also replace the XC3S1000L FPGA (Xilinx, Inc) with the XC3S4000L FPGA since the XC3S1000L FPGA is discontinued.

The new board will have an access panel to the two cochlear implant connectors (one for each ear). This access panel will be mounted on a daughter board, which will have a right angle positioning of the cochlear implant connectors with respect to the SDIO board. This is designed to prevent any accidental detachment of the cochlear connectors from the board. The layout of the new (and final) board has been submitted for fabrication.

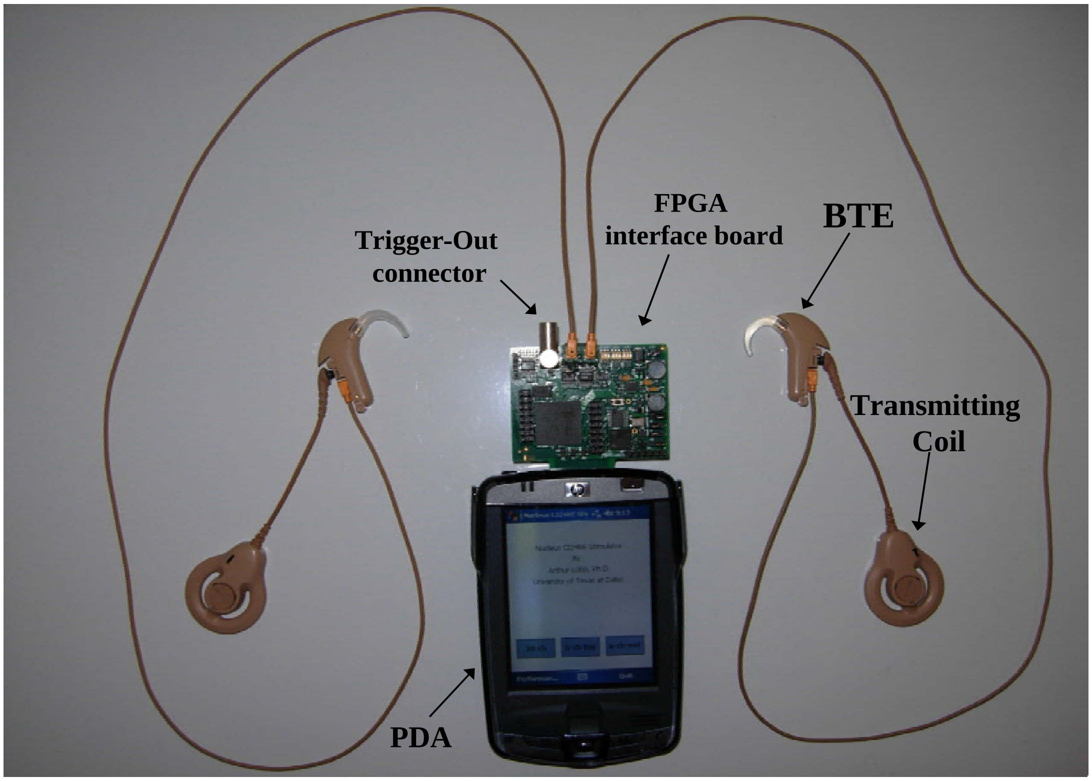

Figure 1. The final prototype PDA implant system consisting of the PDA, SDIO interface board and two BTEs. The BTE units house the microphones.

2.2 Implementation of beamforming algorithm for bilateral applications

A beamforming algorithm was implemented on the PDA to allow researchers interested in bilateral cochlear implant studies to explore variations or improvements to bilateral coding algorithms. More precisely, the Griffiths and Jim (1982) beamforming algorithm was implemented, as shown in Figure 2. The beamforming algorithm operates on the principle that when the target signal comes from the front, the subtracter output at the bottom input (mic 2) should contain primarily noise since the outputs from the two microphones will cancel each other. In contrast, the output of the adder in the top input (mic 1) should contain a mixture of the noise and the signal of interest. These two outputs containing the noisy signal and reference noise signals respectively are fed as input to an adaptive filter shown to the right in Fig. 2. The Least Mean Square (LMS) algorithm is used to adapt the filter coefficients in such a way as to minimize the power of the output error (Fig. 2). The error signal is also the "enhanced" signal that is fed to the input of the cochlear implant device. The above beamforming algorithm (Fig. 2) has been found to work well in situations where there is only one noise source present and there is no reverberation (e.g. Spriet *et al.*, 2007; van Hoesel and Clark, 1995). The beamformer (BEAM) implemented in the Nucleus Freedom processor uses two microphones (front directional and rear omnidirectional) spaced 1.9 cm apart on a single BTE processor (Spriet *et al.*, 2007). Unlike the Freedom's BEAM system, the proposed PDA system (Figure 1) can be used with two microphones placed in each of the two ears. Hence, the two microphones benefit from a considerably larger spatial separation compared to that in the Nucleus Freedom system.

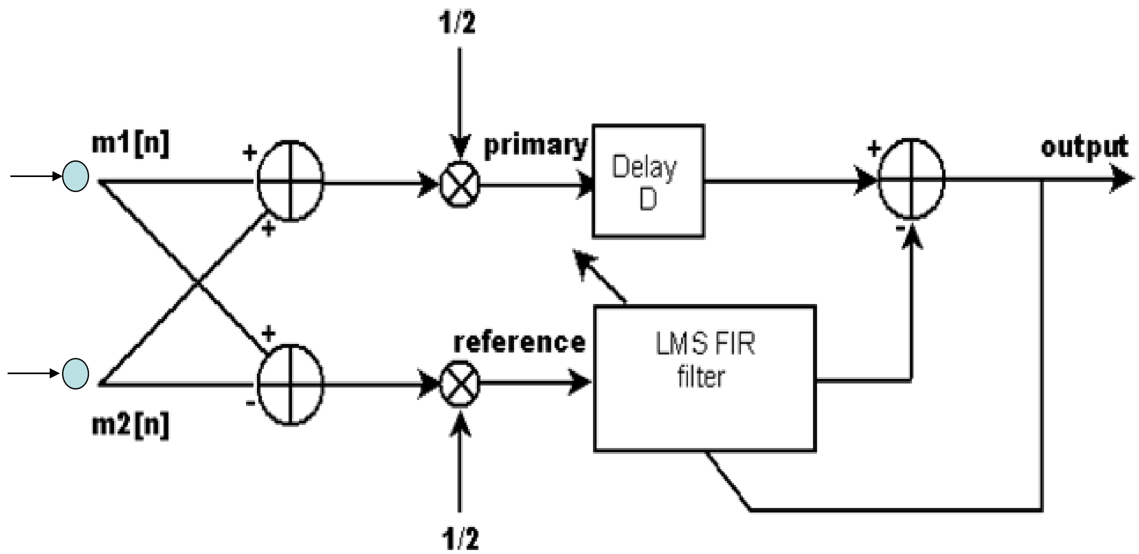

Figure 2: Block diagram of the beamforming algorithm implemented on the PDA. The signals $m_1[n]$ and $m_2[n]$ indicate the two microphone inputs.

A real-time PDA implementation of the beamforming algorithm (Figure 2) was completed. This algorithm can be used as a front end to the ACE algorithm. Profiling of the timing of the algorithm indicated that it can be run real-time using as many as 128 FIR coefficients in the LMS algorithm. This profiling included the time to process the signal through the ACE algorithm. Figure 3 shows an example spectrogram of an output signal processed through the PDA implementation of the beamforming algorithm. The test sentence (taken from the IEEE corpus) was processed through a Head Related Transfer Function (HRTF) to simulate the condition in which the target is located at the front and the noise (masker) is located at 90^o azimuth. The target-to-masker ratio was set to -5 dB and the masker was speech-weighted (steady) noise. For this example, a total of 128 FIR filter coefficients were used in the implementation with a 64-sample delay in the primary path (Figure 2). Comparing the spectrograms in Figure 3 with those in Figure 4 (unprocessed stimuli), we note that the processed signal contained formant transition (F1/F2) information, critical for speech understanding. In the next quarter, we will test the intelligibility of speech processed via the beamforming algorithm with normal-hearing listeners.

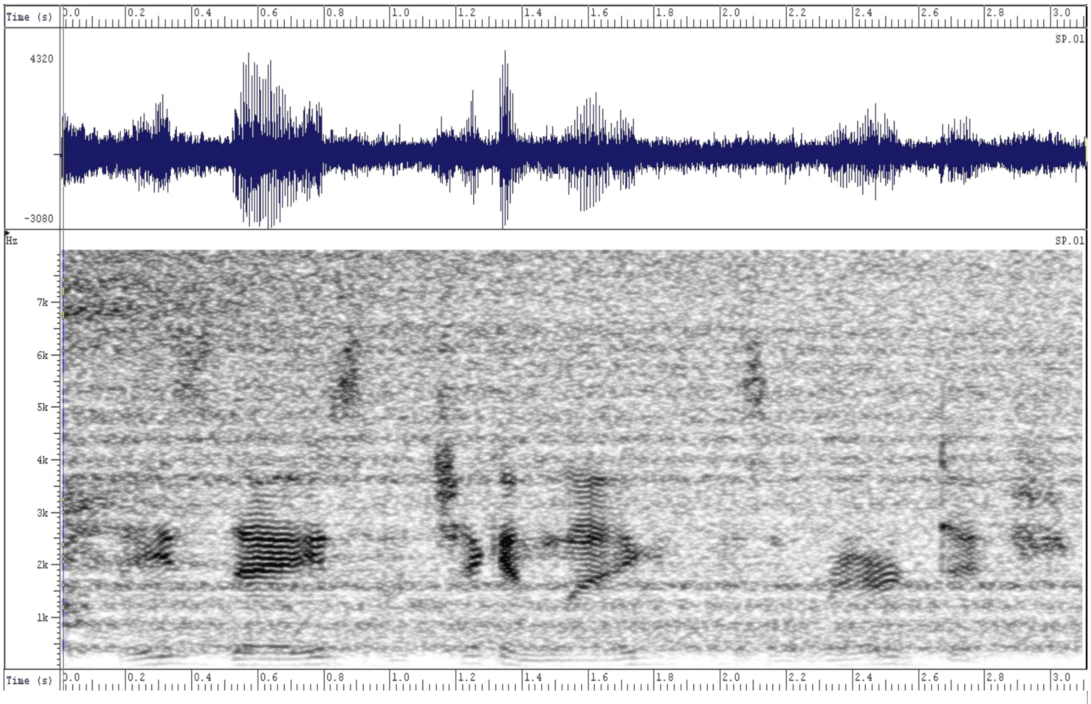

Figure 3. Time-domain waveform (top panel) and spectrogram (bottom panel) of an IEEE sentence processed via the beamforming algorithm implemented on the PDA. A total of 128 FIR filter coefficients were used in the LMS update equation. The input to the algorithm were the sentences (-5 dB target-to-mask ratio) shown in Figure 4, as captured by the two mics.

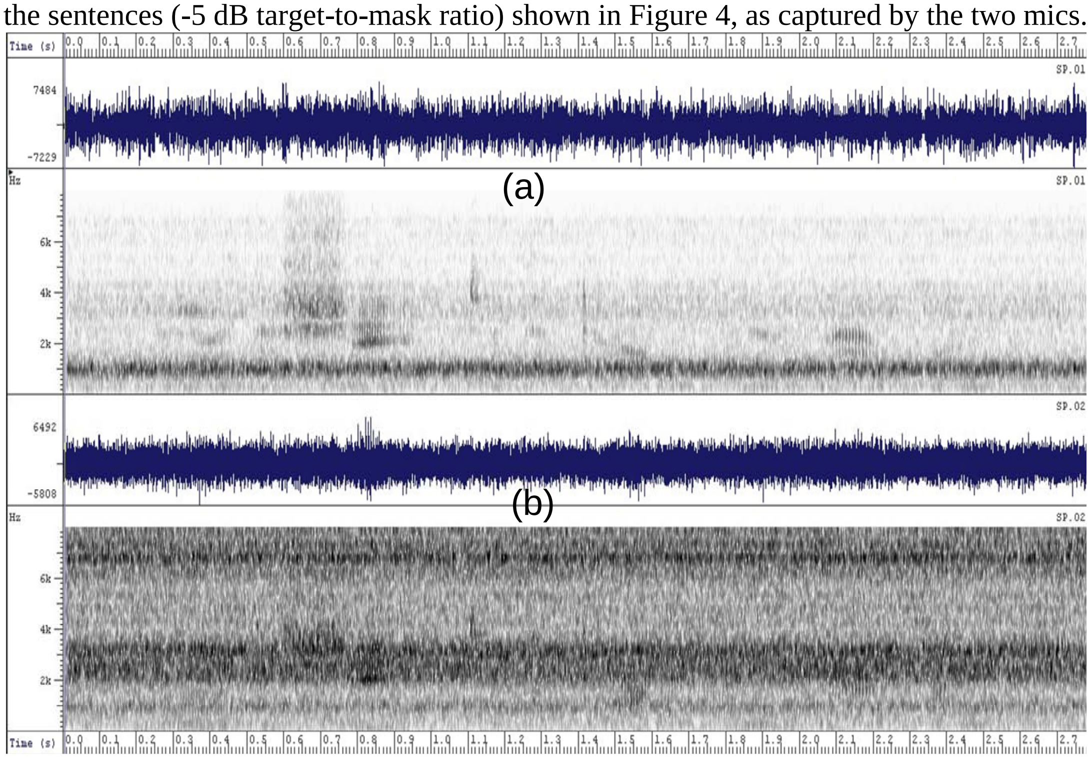

Figure 4. Panel (a) shows the spectrogram of the signal captured in the left ear, and panel (b) shows the spectrogram of the signal captured in the right ear. The target was located at the front and the masker (speech-weighted noise) was located at 90^{o} azimuth (i.e., on the right).

2.3 FFT code optimization

The ACE strategy estimates the incoming signal spectrum using a Fast Fourier Transform (FFT), which simulates a bank of band-pass filters followed by envelope smoothing (Vandali *et al.,* 2000). A 128-point FFT is often used to process the incoming signal in short-term intervals (or frames) following Hanning-windowing of the signal. Depending on the analysis and stimulation rates, there exists significant overlap (in samples) between adjacent frames. This overlap can be exploited to some degree to reduce the number of computations involved in the FFT implementation. In this quarter, we focused on obtaining a real-time implementation of a recursive-based FFT approach on the PDA platform (Amin, 1987). Initially, a floating-point version of the recursive approach was implemented, which was then converted to fixed-point implementation. Much effort was spent to keep the accuracy as close as possible to the floating-point version. The conversion from floating to fixed-point was made possible by keeping the FFT computation in Q15 format and the output of analysis stage at every channel in Q15 format. A real-time implementation of the recursive FFT algorithm was achieved using 128- and 256-point FFTs on the PDA platform.

Profiling was performed to assess the computational savings with different size FFTs. The results are given in Table 1, which shows the time required to process a 46.4 ms frame using the filterbank and the recursive FFT methods on the PDA platform. As seen from this table, the time required to process the signal in the analysis stage using a 128-point FFT was less than half the time required by the filterbank approach (using C DLLs). The analysis stage involves computing the FFT and summing the magnitude square of the frequency bins falling in a particular frequency band. The band outputs from the recursive FFT approach are subsequently smoothed using a low-pass filter to match the analysis output obtained from the filterbank approach. The time required to implement the filterbank approach using Intel's IPP routines is also provided in Table 1 for comparative purposes. The recursive FFT approach requires only 4 real multiplications and additions to compute the FFT at a specific frequency bin, and requires half of the time used by the filterbank approach when the number of FFT points is limited to 128. In the fixed-point implementation of the recursive-based FFT approach, we observed that errors were occasionally introduced in the computation due to finite precision, and those errors propagated when the recursive approach was applied for a long time. To rectify this, we reset the FFT computation every 96 ms. This introduced a small, but non-significant, overhead. The time reported in Table 1 included this overhead.

The recursive FFT implementation of the ACE algorithm did not compromise the accuracy of the envelope amplitudes. Figure 5 shows the electrodogram of the syllable "asa" processed using the recursive FFT implementation (128 points) of the ACE algorithm. For this example, all 22 channel envelope (log-compressed) amplitudes are displayed (i.e., it is a 22-of-22 implementation of ACE).

Processing approach	Filterbank approach using IPP routines	Filterbank approach using LabVIEW with C DLL running on PDA	Recursive FFT using LabVIEW and C DLLs	
			N=128	N=256
Decomposition and envelope detection/ FFT and weighted sum of bin powers	6 ms	20 ms	7 ms	13 ms

Table 1. Comparative profiling results for the implementation of ACE using three different methods. The timing is shown relative to a 46.4 ms input buffer. The recursive-based FFT implementation was done with N=128 point FFT and N=256 point FFT.

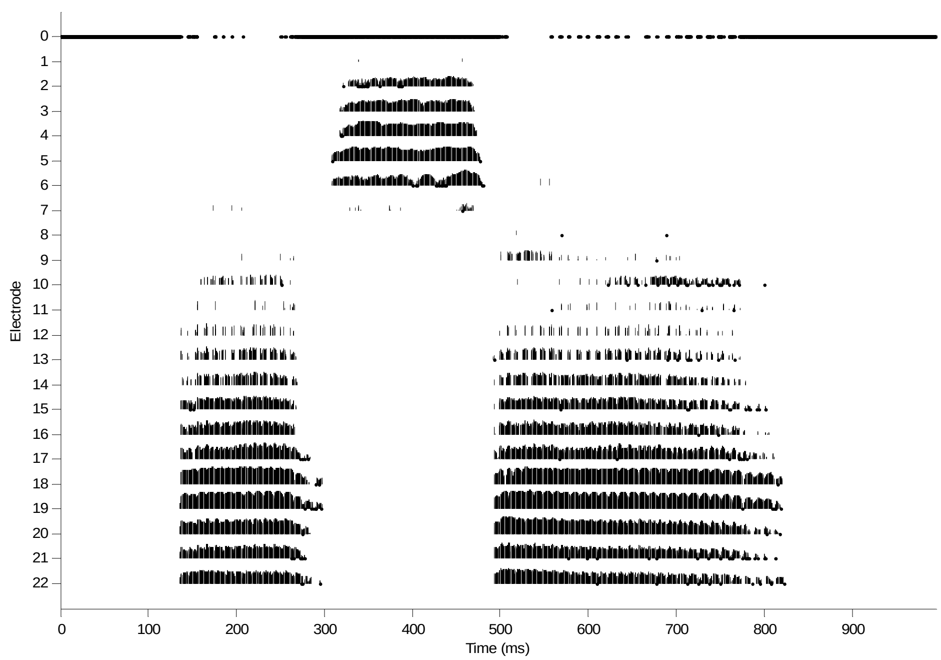

Figure 5. Electrodogram of the syllable “asa” using the recursive-based FFT implementation on the PDA. Envelopes are shown for all 22 channels.

2.4 Other Activities

- Visited Cochlear Corporation (Denver, CO) and presented a real-time demo of the bilateral PDA system (Figure 1).
- Submitted a pre-IDE application to FDA seeking approval of the SDIO interface board.

2.5 Plans for next quarter

- Debug and test the final SDIO interface board.
- Test and debug the multi-channel stimulator IC chip (expected in August).

References

Amin, M. (1987) "A new approach to recursive Fourier transform," *Proc. IEEE*, 75, 1537-1538.

Griffiths, L and Jim, C. (1982). “An alternative approach to linearly constrained adaptive beamforming,” *IEEE Trans Antennas Propagation*,” AP-30, 27-34.

Spriet, A., Van Deun. L., Eftaxiadis, K., Laneau, J., Moonen, M., Van Dijk, B., Van Wieringen, A., Wouters, J. (2007). Speech understanding in background noise with the two-microphone adaptive beamformer BEAM in the Nucleus Freedom cochlear implant system. *Ear and Hearing*, 28, 62–72.

Van Hoesel, R and Clark G (1995). Evaluation of a portable two-microphone adaptive beamforming speech processor with cochlear implant patients. *J Acoust Soc Am*., 97(4), 2498-2503.

Vandali A, Whitford L, Plant K, Clark G (2000). “Speech perception as a function of electrical stimulation rate using the Nucleus 24 cochlear implant system,” *Ear Hear*. 21(6), 608-624.

Appendix

S. Guo, H. Lee and P. Loizou (2008) “A 9-bit configurable current source with enhanced output resistance for cochlear stimulators,” *IEEE Custom Integrated Circuits Conference,* San Jose, CA, Sep. 2008, accepted for publication.