Eighth Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Work in this quarter focused on debugging and testing the SDIO interface board (v.2). We successfully tested the signal acquisition stage of the board. The acoustic signal is captured by the microphone located in the Cochlear Corporation's BTE headset, and sent to the PDA for processing. The new board allows for the acquisition of binaural inputs from the two microphones (one in each ear) embedded in the BTEs. We also tested the generation of a trigger signal (5 V) that can be used for synchronization purposes in external ECAP/EABR recording systems. Finally, we report improvements to the filtering routines implemented on the PDA. The new filtering routines, crucial for the operation of CIS algorithms, produce smaller quantization error.

2.1 SDIO interface board (version 2) – Signal acquisition

Much effort was spent in debugging and testing the new SDIO interface board (v.2). As mentioned in the last quarterly report (QPR7), the new interface board (v.2) extends the capability of the first board in that it allows for the acquisition of binaural inputs from the two microphones (one in each ear) embedded in Cochlear Corporation's BTE headset. Subsequently, it can be used for simultaneous stimulation of bilateral implants. We completed testing the signal data acquisition component of the new board (see Figure 1).

We initially encountered some problems with the data acquisition circuit, as we noted that the acquired signal was clipped. This is now fixed, and we summarize next the steps we took to rectify the signal acquisition issues. The LTC6912 preamplifier is powered by a single rail 3.3 V supply and expects an input swing between +1.65 V and -1.65 V centered at 1.65 V. That is, with no AC input, 1.65 V DC should appear at the input. When the SDIO v.2 board was received, the zero-AC-input voltage at the preamplifier input was 400 mV and as a result the acquired signal was being clipped and appeared as a half-wave rectified waveform. One of the input capacitors bypassing the analog ground to ground was shorted pulling the DC bias to the low value. The capacitor was replaced restoring the DC bias at the input to the preamp to 1.65 V. Another aspect of the dynamic range is that the LTC1407A ADC can accept differential signals in the range of +/- 1.25 V. With the negative input initially tied to analog ground, the input was appearing at +1.65 V all the time. It was only when the AC part of the test waveform dropped below 1.25 V that part of the waveform was seen. The rest of the time the input was saturated. The potential divider was adjusted at the input to the ADC to get the best dynamic range at the input to the ADC. The LTC6912 analog ground and the LTC1407A negative input now are at 2.1 V and the input signal can swing between +1.2 V and –2.1 V instead of between +1.65 V and -1.65 V. This provided a ~0.5 V gain in dynamic range compared to the previous biasing mechanism. The headroom below -1.25 V is not used. Figure 2

shows a sample recording of a sustained production of the vowel /a/ made using the signal acquisition circuit on the SDIO Interface board.

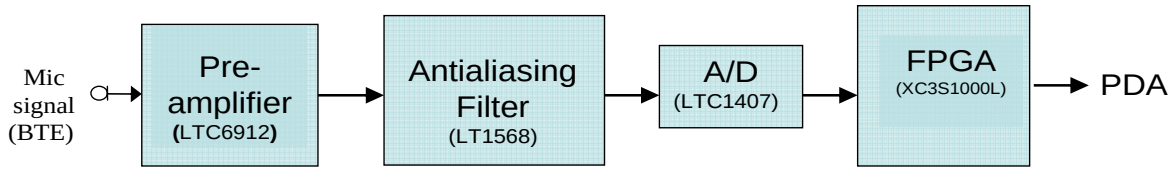

Figure 1. Signal data acquisition diagram for SDIO board (v. 2).

The acoustic signal is now captured by the HS8 microphones embedded in the L and R BTEs (Cochlear Corp.). The signal in each channel is pre-amplified by the LTC6912 preamplifier with one of 8 gain settings 0, 1, 2, 5, 10, 20, 50 and 100 corresponding to -120 dB, 0 dB, 6 dB, 14 dB, 20 dB, 26 dB, 34 dB and 40 dB. The output of the preamplifier is filtered by the LT1568 anti-aliasing filter IC configured as a dual second-order Bessel filter with a cutoff frequency of 11,025 Hz. The output of the anti-aliasing filter is sampled by the 14-bit LTC1407A ADC at 22 kHz and sent to the FPGA master over an SPI interface. The FPGA buffers 256 samples/channel for the L and R channels and sends the data every 11.6 ms to the PDA via the AC2600 SDIO target controller. The transfer is initiated by a PDA-issued Read interrupt. The PDA receives the microphone sample payload in a thread, processes it with CIS-16 or ACE strategies binaurally and transmits the stimulus amplitudes for the L and R channels in the same thread to the FPGA via the write interrupt. The FPGA receives the amplitudes, encodes them in Embedded Protocol (EP) and transmits the encoded bits with 5 MHz On-Off Keying modulation to the L and R Nucleus Freedom coils. There is no propagation delay for stimulus pulses sent to the L and R channels since both coils receive corresponding EP transmissions in the same 5-MHz clock cycle.

In addition to the data acquisition testing, we also tested the 5V trigger out pulse from the board. A 5V trigger signal was successfully generated from the FPGA and a single-bit dual-supply bus transceiver. The latter translates between 3.3V and 5V logic levels. The trigger signal can be used for synchronization purposes in external ECAP/EABR recording systems. The total amount of current drawn by the board for combined stimulation and triggering is 130 mA. The FPGA boot from the Xilinx Platform Flash PROM on power cycling has also been tested, making the download of the bit file via the JTAG interface unnecessary.

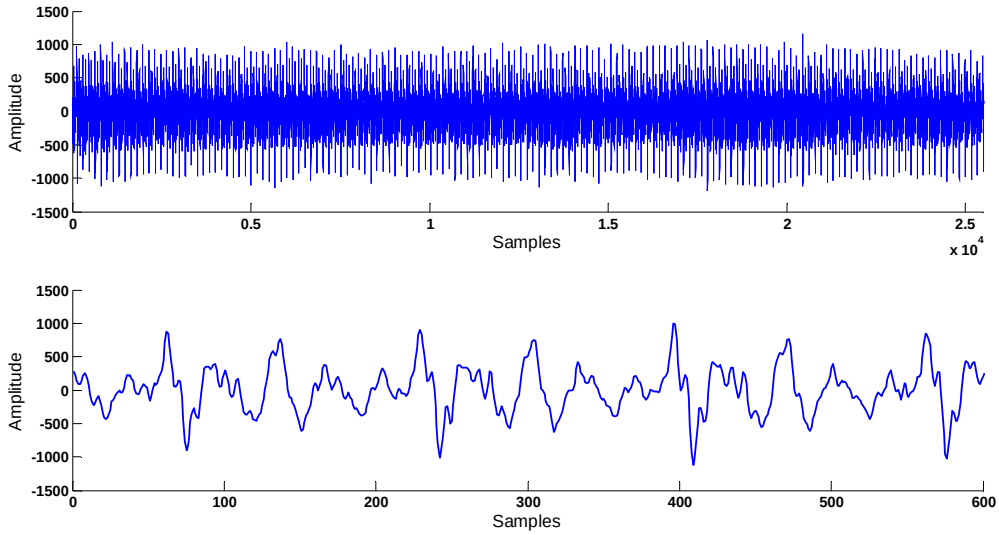

Figure 2. Sample recording of a sustained production of the vowel /a/ made using the A/D chip on the SDIO-interface board (Fig. 1). Top panel shows the sampled (at 22 kHz) waveform of the vowel /a/ (duration =1.1 secs), and bottom panel shows a zoomed display of 600 samples of the vowel /a/ taken from the middle portion of the recording.

2.2 Improving filtering accuracy

The filtering operation is critical in the implementation of the CIS speech-coding algorithm. The existing filtering routine provided by Intel (in their IPP library) has limited precision (16-bits). The bandpass filtering (BPF) implementation uses 3 bi-quad sections for the realization of 6-tap IIR filters. Sixteen-bit precision is used for the storage of filter coefficients, intermediate section outputs, and for the filter state variables. The IPP filtering routine was optimized in assembly language for the ARM9E architecture.

As the 32-bit registers in the ARM9E architecture limit the maximum precision that can be obtained with 16-bit filter coefficients, the accuracy is limited accordingly. The precision can be improved; however, by exploiting the vector processing (Single Instruction and Multiple Data, SIMD) capability of the PXA27xx processor (used in most PDAs) and by using 64-bit registers. This allows for improvement of the precision of the filter implementation (in terms of lower quantization error) without additional cost of complexity. Hence, BPF filtering in CIS is upgraded now to use 24-bit filter coefficients and 32-bit resolution for the filter-state and intermediate outputs of the bi-quad sections.

To quantify the reduction of quantization error brought with the 24-bit implementation, we computed the normalized mean-square error (MSE) between the floating-point filtered output and the 24-bit and 16-bit filtered outputs. The normalized MSE in channel *i* was computed as follows:

$$MSE(i) = \frac{\sum_t \left(Y^i_{FLT}(t) - Y^i_{PDA}(t)\right)^2}{\sum_t \left(Y^i_{FLT}(t)\right)^2} \quad (1)$$

where $Y^i_{FLT}(t)$ denotes the floating-point filtered waveform in the *i*th channel, and $Y^i_{PDA}(t)$ denotes the PDA filtered waveform obtained using 16-bit or 24-bit implementations. Table 1 tabulates the MSE values for 16 channels obtained using as input one sentence from the IEEE corpus. Consistent reduction in MSE is noted for all channels with the 24-bit implementation. Figure 3 compares the

filtered waveforms obtained with 16-bit, 24-bit and floating point implementations for the same sentence. Only the waveforms for channels 1 (center frequency=330 Hz), 8 (CF=1100 Hz) and 13 (CF=3000 Hz) are shown. As can be seen the 24-bit filtered waveforms follow closely the floating-point waveforms.

Channel	MSE 16-bit coefficients	MSE 24-bit coefficients
1	**0.4769**	**0.2507**
2	**0.4818**	**0.2507**
3	**0.7470**	**0.2505**
4	**0.7538**	**0.2505**
5	**0.6933**	**0.2509**
6	**0.7092**	**0.2511**
7	**0.9218**	**0.2506**
8	**0.9500**	**0.2508**
9	**0.9095**	**0.2522**
10	**0.6832**	**0.2549**
11	**0.6500**	**0.2561**
12	**0.7284**	**0.2551**
13	**0.6526**	**0.2528**
14	**0.8314**	**0.2524**
15	**0.6555**	**0.2580**
16	**0.5172**	**0.2574**

Table 1. Comparison of MSE values between 16-bit and 24-bit bandpass-filter implementations for different channels. Smaller MSE values indicate smaller quantization error.

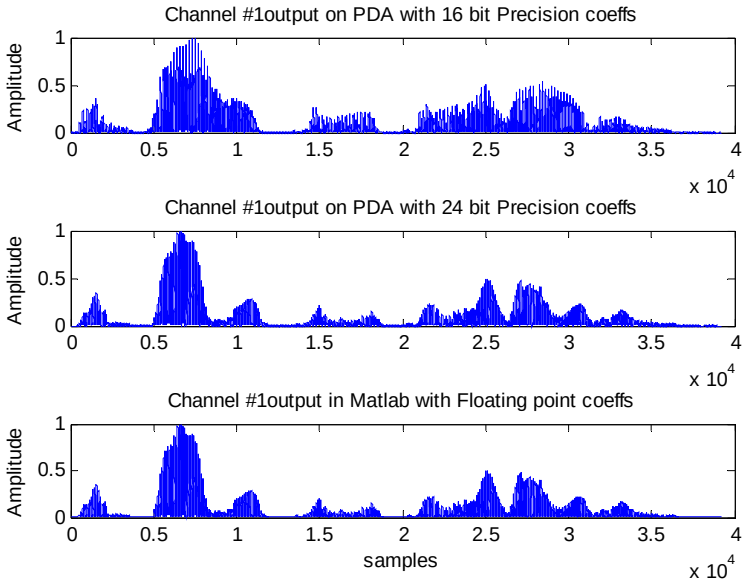

Figure 3. Bandpass-filtered waveforms for channel 1 obtained using floating-point implementation (bottom panel), and 16- and 24-bit implementations (top two panels).

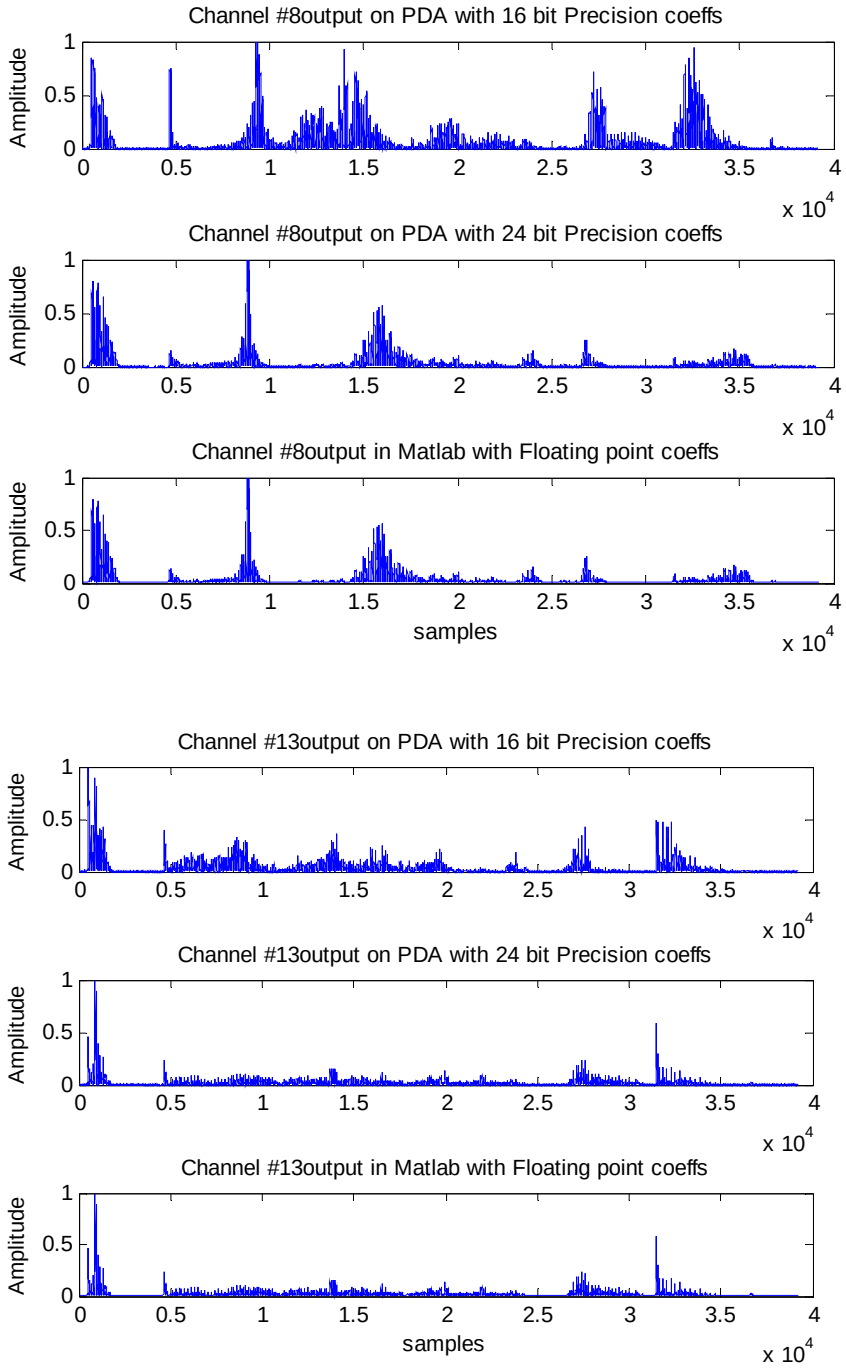

Figure 3 (cont-ed). Bandpass-filtered waveforms for channels 8 and 13 obtained using floating-point implementation, and 16- and 24-bit implementations.

2.3 Plans for next quarter

- Continue testing and debugging the SDIO interface board (v. 2).
- Visit Cochlear Corporation (Denver, CO) to seek feedback about our PDA interface board.
- Prepare a pre-IDE application to FDA.