Seventh Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Work in this quarter focused on completing the hardware design of an 8-channel stimulator which can be used for animal studies. This stimulator has the capability of providing simultaneous stimulation to eight electrodes. Simulation results are presented in this quarter. The SDIO interface board (version 2) was received and is currently being tested and debugged. The new interface board (v.2) extends and enhances greatly the capability of the first board in the following ways: (1) allows for the acquisition of binaural inputs from the two microphones (one in each ear) embedded in Cochlear Corporation's BTE headset, (2) can provide access to an external trigger signal that can be used for ECAP/EABR recording systems (3) allows for simultaneous and/or coordinated stimulation of bilateral implants, and (4) allows for the possibility of backward telemetry and development of diagnostic software tools. The software design and signal flow of the data acquisition component is presented in this quarter. Lastly, a comprehensive User's Guide for the LabVIEW implementation has been completed.

2.1 Development of an eight-channel stimulator for animal studies

A new eight-channel current stimulator capable of performing either simultaneous or sequential stimulation has been designed using AMS (Austriamicrosystems) 0.35μm CMOS process. Fig. 1 shows the block diagram of the new current stimulator, which consists of eight independent current sources with each current source being capable of sourcing or sinking output current pulses of 1mA with 9-bit current-amplitude resolution. The biphasic current pulses (anodic and cathodic phases) from each channel are independently controlled by two inputs Ctrl1 and Ctrl2 to ensure charge-balanced stimulation. In addition, the current source in each channel has its own current-amplitude controller to provide independent amplitude control. Moreover, a channel selector takes 3-bit channel information to provide different types of stimulation modes including simultaneous, sequential or combinations of the two.

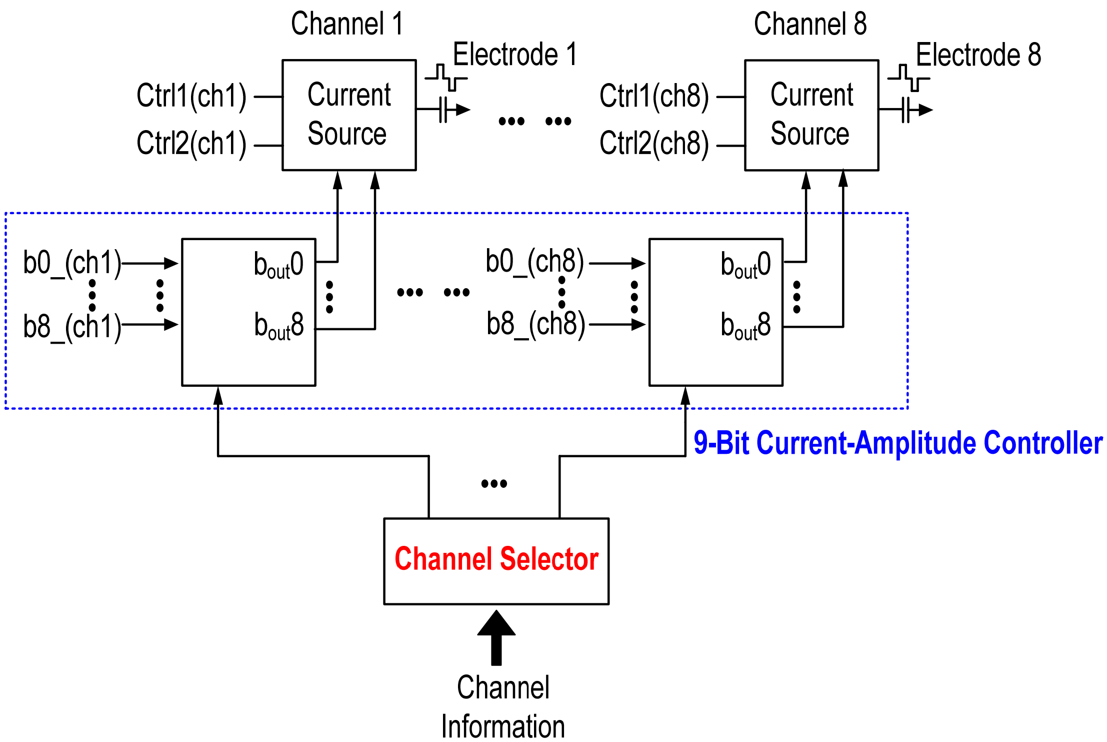
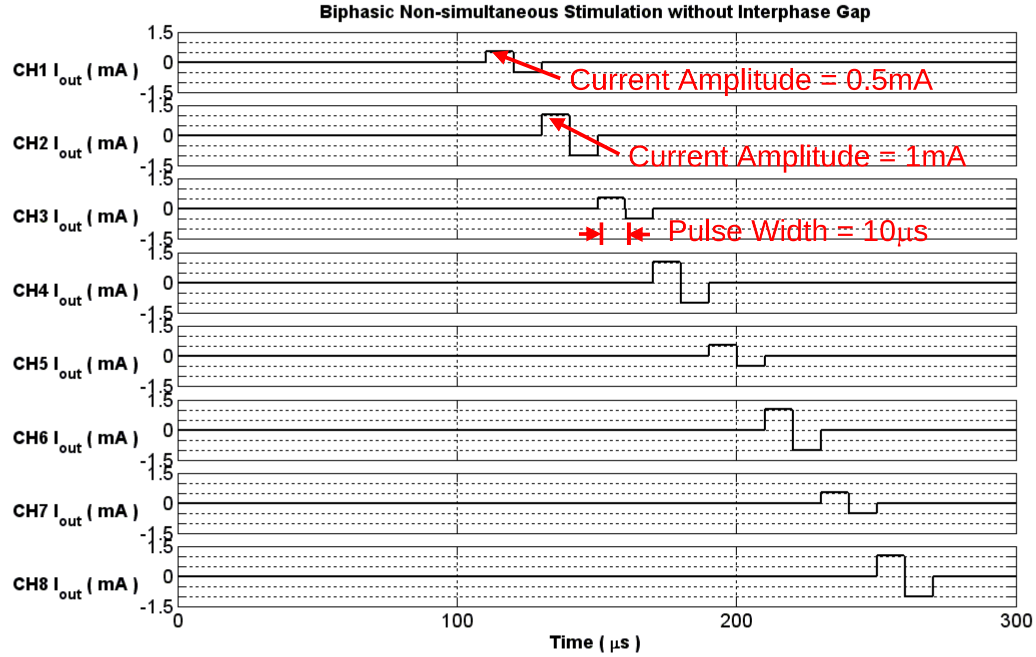


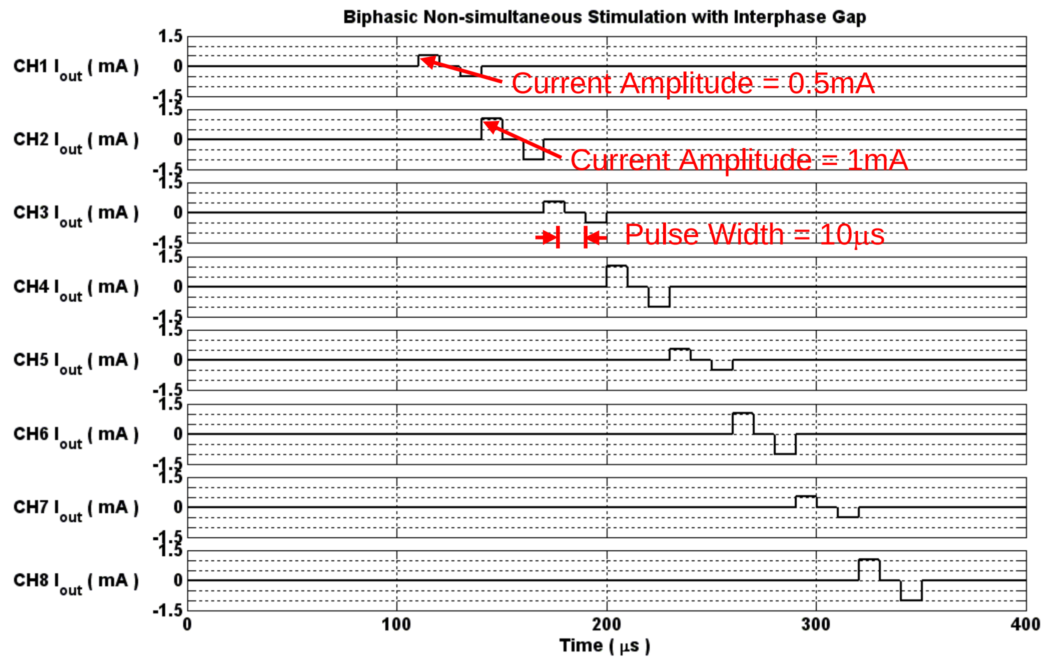
Figure 1. Structure of the eight-channel current stimulator.

To verify the functionality of the new current stimulator, circuit simulations were run to generate charge-balanced biphasic current pulses in different stimulation modes. Figs. 2 (a) and (b) show simulation results of the output currents in eight different channels under non-simultaneous conditions. The current amplitude and pulse width of current pulses in each channel can be controlled independently. For this example, the current amplitude of odd-number channels and even-number channels were set to 0.5mA and 1mA respectively, and the pulse width of either anodic or cathodic current pulse was set to 10μs. Results from Figs. 3(a) and (b) also indicate that the new stimulator is able to generate anodic and cathodic current pulses with or without a controllable inter-pulse shorting. Moreover, both Figs 2(c) and (d) show that charge-balanced biphasic current pulses in each channel can be generated with or without inter-pulse shorting under the simultaneous stimulation mode.

Table I provides the performance summary of the new stimulator. With a 5V supply voltage, a high compliance voltage of 4.65V can be achieved in the current source of each channel. The minimum pulse width of the current pulse is 1μs, which allows the stimulator to provide high stimulation rates.

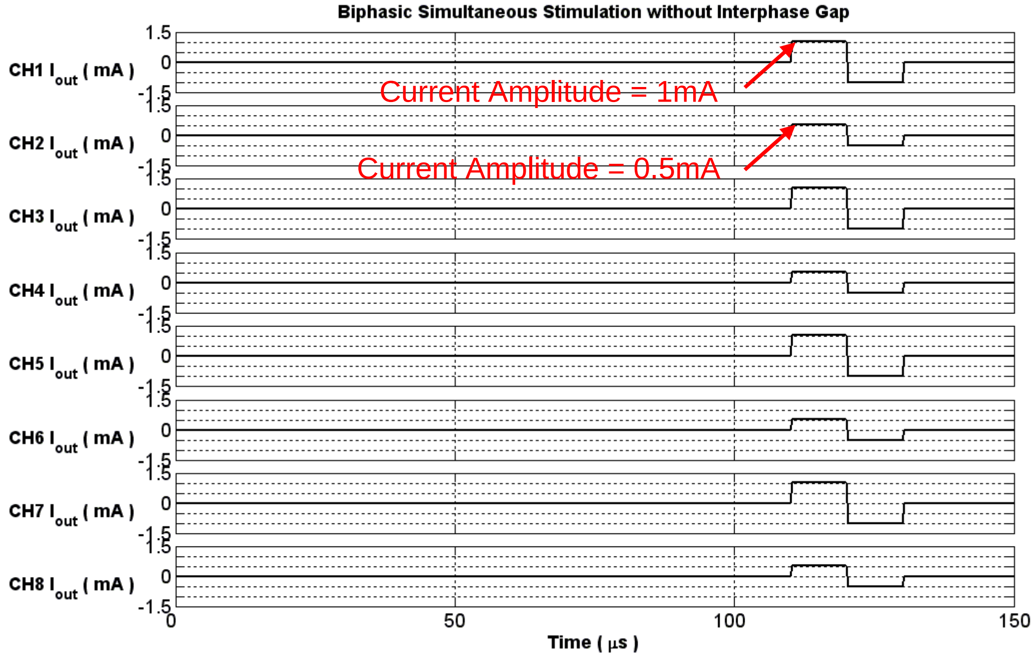


(a)

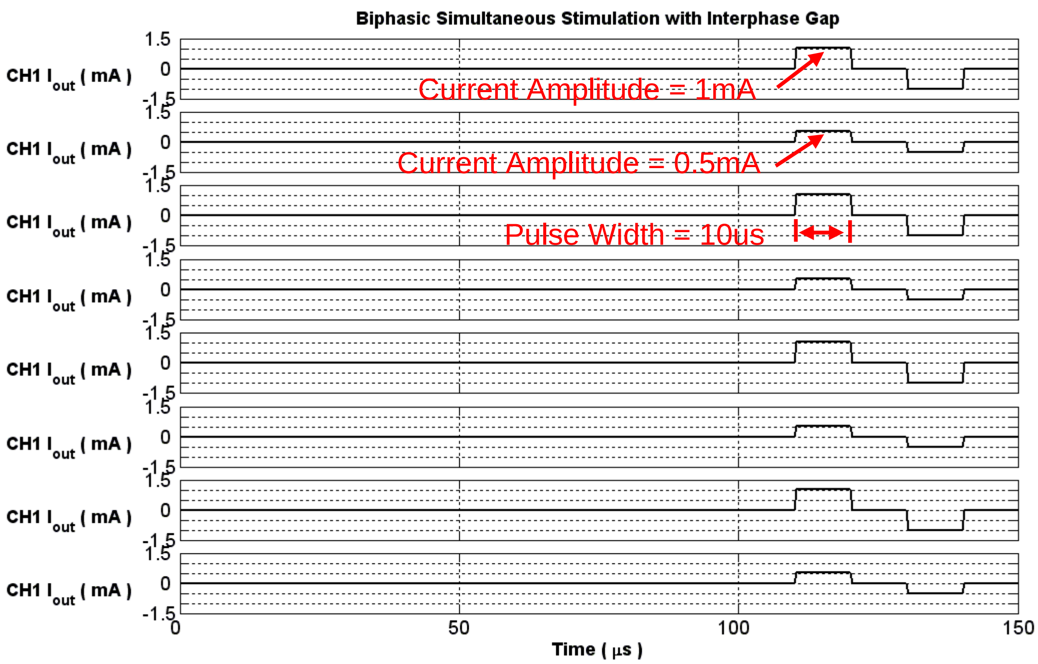


(b)

Fig. 2. Simulated output current pulses used for biphasic non-simultaneous stimulation (a) without inter-phase gaps and (b) with inter-phase gaps.



(a)



(b)

Figure 3. Simulated output current pulses used for simultaneous stimulation (a) without inter-phase gaps and (b) with inter-phase gaps.

Table I Performance Summary of 7-channel Stimulator

Supply Voltage	5V
Per Channel Power Consumption	5mW@5V
Compliance Voltage	4.65V
Biphasic Stimulation Levels	1mA (9-bit resolution)
Minimum Pulsewidth	<1μs
Technology	AMS 0.35μm CMOS (4 metals & 2 poly layers)

2.3 SDIO interface board (version 2)

The new SDIO interface board (v. 2) has been received (see Figure 4) and is currently being tested. The new interface board (v.2) extends the capability of the first board in that it allows for the acquisition of binaural inputs from the two microphones (one in each ear) embedded in Cochlear Corporation's BTE headset. Subsequently, it can be used for simultaneous stimulation of bilateral implants. We describe next the signal data acquisition component of the new board.

Figure 4. Picture of the SDIO interface board (version 2).

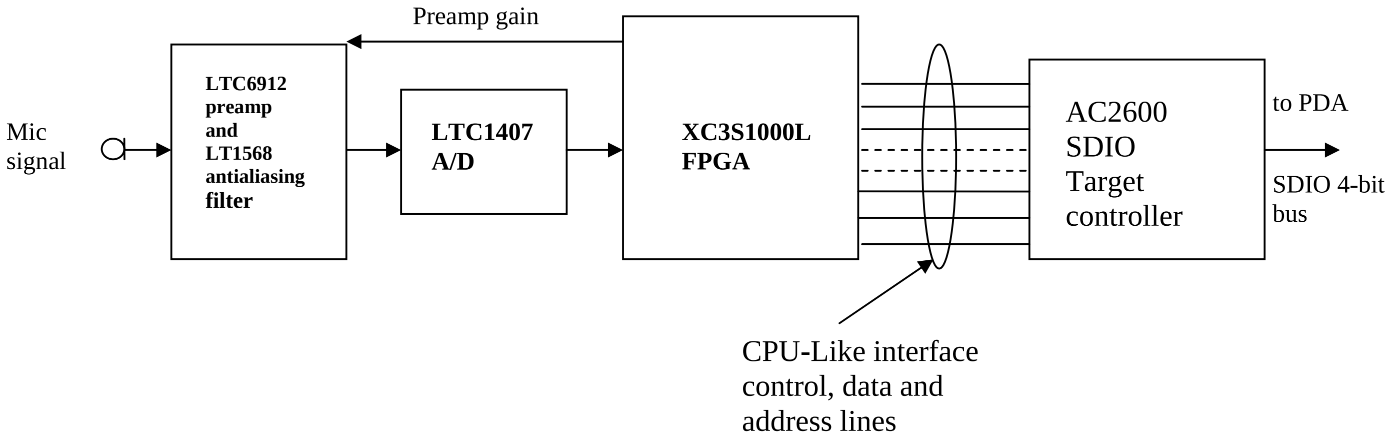


Figure 5. Signal data acquisition diagram for SDIO board (version 2).

Figure 5 shows the data path from the microphone to the PDA for a single channel. The microphone signal is first pre-amplified and antialiasing-filtered before being sampled by the LTC1407 A/D. The FPGA has a Receive (from A/D) state machine (SM) running in parallel with the Transmit-to-PDA SM operating at a 60-MHz clock from the AC2600 ASIC. The Receive (from A/D) SM initializes the preamplifier gains before acquiring samples from the A/D. The incoming samples are buffered and transferred to the AC2600 in 16-bit parallel mode via the CPU-Like interface. The CPU-Like interface consists of the control, data and address lines which are asserted when a specific SDIO command is issued by the PDA. The Transmit-to-PDA SM is driven by an FPGA-generated interrupt to the AC2600 using the CPU-Like interface. When the interrupt from the FPGA is detected, the PDA reads the FPGA interrupt status register to determine the interrupt type and then finally issues the appropriate command to read or write the data. The above implementation accommodates bidirectional data transfers to/from the electrodes. That is, it accommodates a PDA-to-FPGA-to-electrode data transfer (i.e., for electrical stimulation) and a mic-to-FPGA-to-PDA data transfer (i.e., for microphone signal acquisition). Furthermore, it accommodates an electrode-to-FPGA-to-PDA data transfer for reverse telemetry. That is, it can be used for receiving electrode impedances and collecting compound action potentials from electrical stimulation.

2.3 User's Guide

A user's guide describing the LabVIEW software implementation of the CIS strategy and noise-band vocoder for both PC and PDA platforms was written. The user's guide provides an overview of the modules involved and describes the input parameters available to the user as well as the outputs that are provided by the software. Three different versions are covered in the user's guide. LabVIEW hybrid programming is used in all three versions. These versions are outlined below:

1. CIS Simulator (noise-band vocoder) on PC Platform
   This version corresponds to the CIS cochlear implant signal processing running in real-time on a PC platform. There are four main modules in this version that are explained in the user's guide. These modules include: design of filter coefficients, initialization of filter coefficients, processing of speech signal captured by a microphone, and halting the program. The user's guide also contains a brief explanation of the procedure to build a C DLL, how to call a C DLL from LabVIEW, and a description of all the functions used in the C DLL.
2. Fixed-point CIS Simulator on PC Platform
   This version corresponds to the CIS cochlear implant signal processing utilizing fixed-point filter coefficients running in real-time on a PC platform. The modules that differ in the above floating-point version are explained in the user's guide. These modules include: design of filter coefficients and processing of speech signal using C DLLs. The user's guide provides an explanation as to how the filter coefficients are quantized and how to avoid overflows.
3. CIS Real-Time Fixed-point Implementation on PDA Platform
   This version corresponds to the actual CIS cochlear implant signal processing which can be potentially used for cochlear implant users. The user's guide provides an explanation of the modules that differ from the corresponding modules contained in the PC version and includes the design of filter coefficients and processing of speech signals using the C DLLs. The user's guide provides an explanation as how to build a C DLL for a PDA platform. A listing of various LabVIEW subVIs and the functions used in the C DLL is provided. The procedures used to create a LabVIEW project for PDA and build a corresponding application for PDA are also explained.

2.4 Other activities

We presented the following paper in the *IEEE Dallas Engineering in Medicine and Biology Workshop* held in Richardson, TX in November, 2007:

- Ramachandran, R. and Loizou, P. (2007). "Real-time pitch detection on the PDA for cochlear implant applications," *IEEE Dallas Engineering in Medicine and Biology Workshop*, Richardson, TX, November 11-12, 2007.

2.5 Plans for next quarter

- Following the pre-defined fabrication schedule of AMS 0.35μm CMOS process in the year 2008, we will be sending our 8-channel stimulator design for chip fabrication in the next quarter.
- Continue testing and debugging the SDIO interface board (version 2).

Appendix

Ramachandran, R. and Loizou, P. (2007). "Real-time pitch detection on the PDA for cochlear implant applications," *IEEE Dallas Engineering in Medicine and Biology Workshop*, November 11-12, 2007.

Gopalakrishna, V., Peddigari, V., Kehtarnavaz, V., and Loizou, P. (2008). *User's Guide: Cochlear implant signal processing for the PC and PDA platforms using LabVIEW.*