

Sixth Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Much effort was placed in this quarter on refining and improving the accuracy of the fixed-point implementation of the noise-band vocoder on the PDA platform. As we plan to distribute implementations of commonly used speech coding algorithms (e.g., CIS and ACE) with the PDA platform, we started working on the implementation of the ACE algorithm on the PDA. This implementation follows closely to Cochlear Corporation's implementation. Finally, several changes were made to the SDIO interface board and submitted for fabrication.

2.1 Improving accuracy of fixed-point implementation of noise-band vocoder on PDA

Further investigations were carried out to improve the accuracy of the fixed point LabVIEW implementation of the noise-band vocoder on the PDA platform. More precisely, changes were made to the filter design stage to improve the reliability and accuracy of the filtering operation. Furthermore, new scaling techniques were adopted to limit occasional overflows. The bandpass filters designed using LabVIEW on the PDA platform are based on a cascade of fourth-order filter sections. Thus, to further improve the stability and accuracy of the filtering operations on the PDA platform, the fourth order sections were converted to second-order sections as shown in Fig. 1. An interactive front panel was also designed for the noise-band vocoder to allow users to change the filter order, the filter type, and envelope cutoff frequency (see Fig. 2).

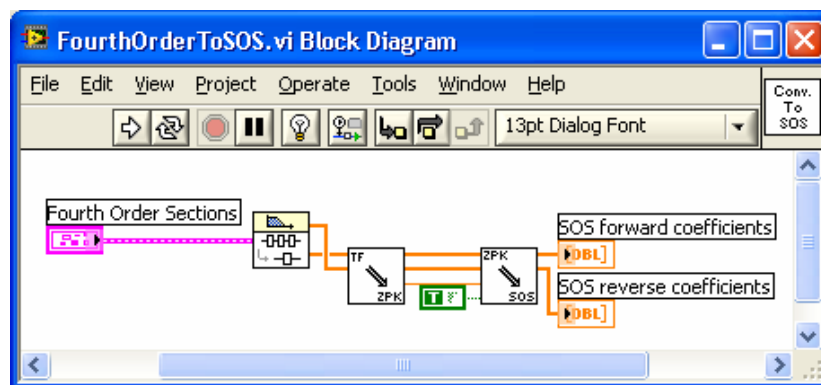


Figure 1. Sub-VI for converting fourth-order sections to second-order sections (SOS) structure.

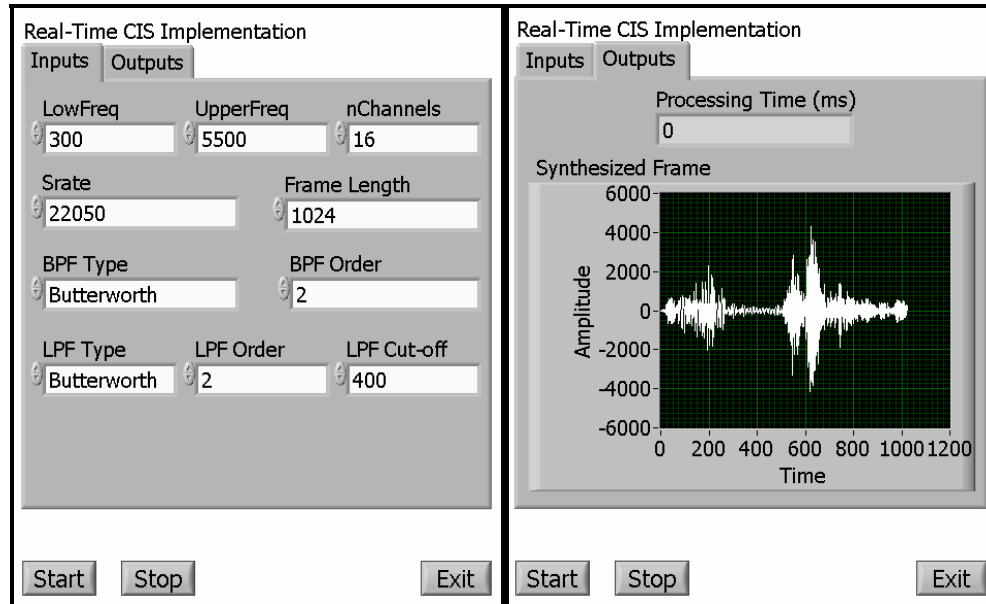


Figure 2. An interactive Front Panel of the noise band vocoder on the PDA.

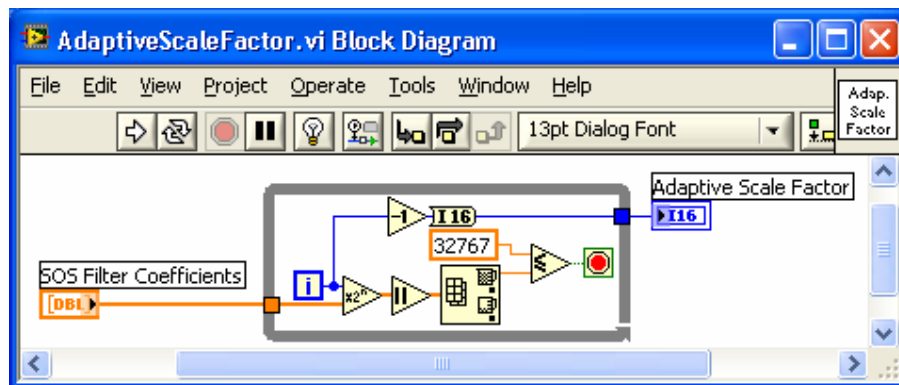


Figure 3. Sub-VI for computing adaptive scaling factors needed to convert floating point coefficients to fixed point coefficients.

Occasional overflows occurred with the LabVIEW implementation when a fixed scaling factor was used to convert the floating point coefficients to fixed point coefficients. This resulted in loss of accuracy for the fixed point implementation. In order to avoid overflows, adaptive scaling factors were introduced which ensured that the values of the fixed point coefficients fell within the allowable range of 16-bit data representation. Fig. 3 shows the Sub-VI used to determine the adaptive scaling factors for a given set of floating point filter coefficients. The newly designed filter coefficients consist of a cascade of second-order filter sections, known to be less sensitive to quantization.

Following the above modifications made to address the occasional overflow issues, the fixed point implementation of the noise band vocoder was compared to the floating point implementation. Fig. 4 shows a sample synthesized speech signal obtained using fixed-point and floating point arithmetic. As can be seen, the synthesized speech obtained using the fixed-point version is nearly identical to that obtained using the floating-point version with a negligible mean squared error (MSE) of 0.000019. Similar MSE values were obtained for other speech samples.

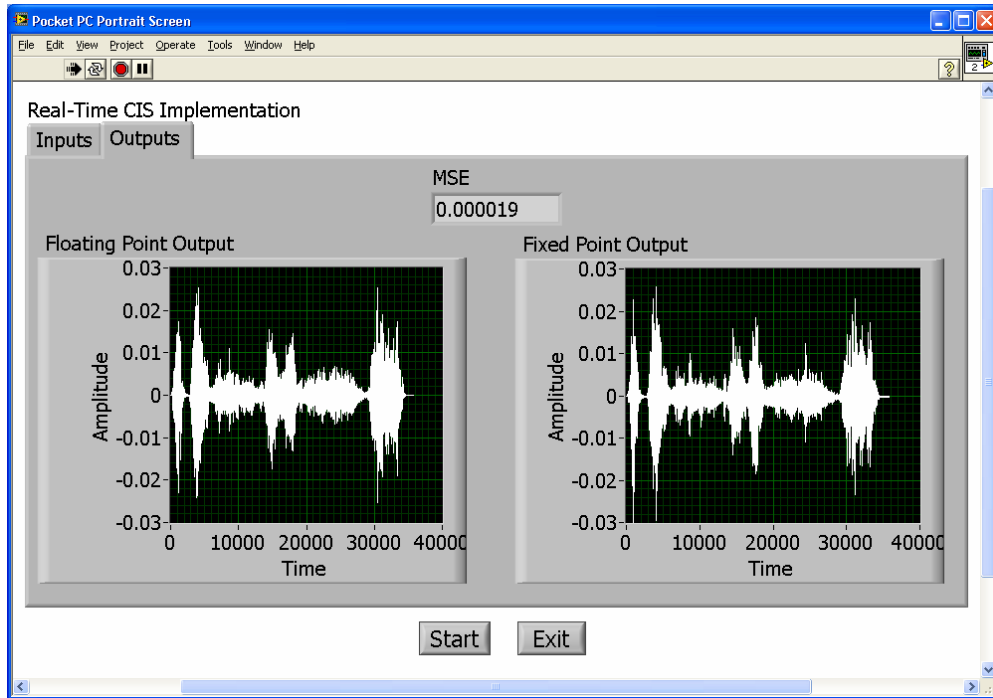


Figure 4. Comparison of synthesized speech obtained using floating-point and fixed-point arithmetic along with the MSE value for a sample IEEE sentence.

In summary, the accuracy of the fixed point implementation was improved by using adaptive scaling factors for the conversion of floating point coefficients to fixed point coefficients. The occasional overflow issue caused by the use of fixed scaling factors was successfully resolved. With the use of adaptive scaling factors, the accuracy of the fixed point version improved significantly and was nearly identical to the floating point version for both noise band vocoder and evoked potential implementations.

2.2 ACE implementation

The Advanced Combination Encoder (ACE) speech processing strategy commonly used in Nucleus-24 implant devices was implemented in C on a Windows Mobile 5.0 PDA. In the following, we describe the implementation steps involved.

Signal is initially buffered in 1024-sample (46.4 ms at 22 kHz sampling rate) frames, which we denote as “super” frames. Subsequent processing is done in 128-sample sub-frames, while applying a block shift of 9 samples on each super frame. The total number of sub frames processed per super frame is 114.

For each sub frame the following processing is done:

1. Apply a Blackman window.
2. Perform a 128-point FFT of the windowed sub-frame using the IPP FFT routine (ippsFFTFwd_RT0CCS_16s32s_Sfs).
3. Compute the square of the FFT magnitudes.

4. Compute the weighted sum of bin powers for 22 channels. The resulting output vector contains the signal power for each of the 22 channels. The zeroth, first and 64th magnitudes (Nyquist component) are not included in the sum.
5. Compute the square root of the weighted sum of bin powers.
6. Sort the 22 channel amplitudes obtained in step (5) using the shell sorting algorithm.
7. Select the n (of 22) maximum channel amplitudes, and scale appropriately the selected amplitudes.
8. Compress the n selected amplitudes using a loudness growth function given by the equation: $y = \frac{\log(1 + \beta \cdot x)}{\log(1 + \beta)}$
where $\beta = 61.47$. A 2048-sample loudness function was generated and stored.
9. Convert the compressed amplitudes, y (Step 8), to current levels as follows:
$$I = (C - T) \cdot y + T$$
where I denotes the current level, T denotes the threshold level and C denotes the most-comfortable loudness level.

Figure 5 shows as an example the electrodiagram of the syllable /a s a/ processed by an 8-of-22 ACE strategy. Lower numbers (1,2, ..) on the y-axis represent basal electrodes and high numbers (..,21, 22) represent apical electrodes.

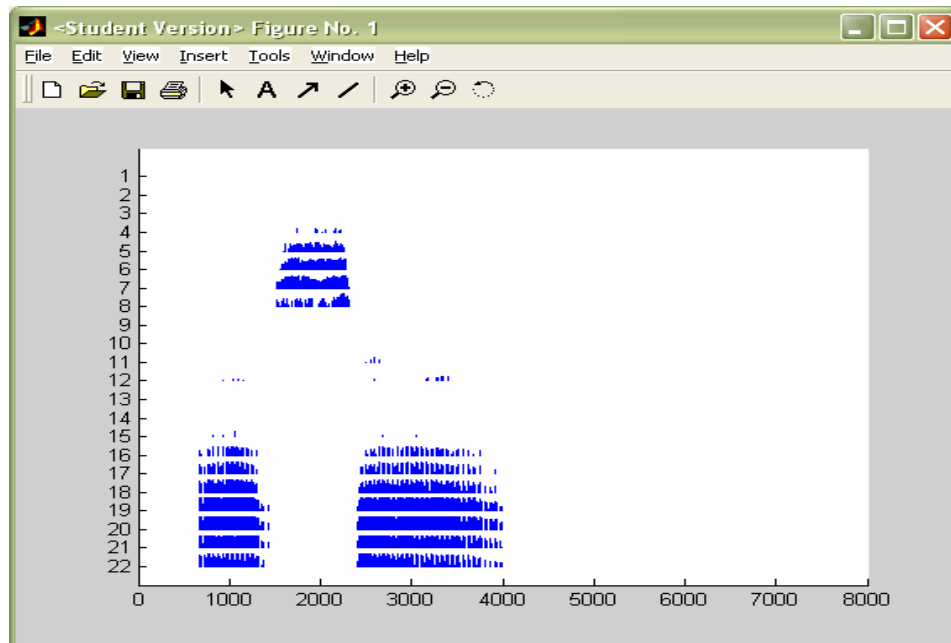


Figure 5. Electrodiagram of the syllable /a s a/ obtained from the ACE algorithm on the PDA. The x-axis labels denote samples, and the y-axis denote envelope amplitudes (in current levels).

Table 1 shows the profiling outcome for the signal processing blocks involved in the ACE implementation. The profiling was measured for a block shift of 9 samples and therefore

applies to a specific stimulation rate. The timing will possibly change for other values of block shifts and stimulation rates. Overall, our ACE implementation on the PDA is done 8.3 times faster than real-time.

Function	Time (μ S)/128 sample sub-frame (Fs=22.05 kHz)	Time (ms)/46.4 ms super frame with block shift =9 samples
Windowing	6.83	0.78
FFT	9.80	1.12
Squared magnitude	2.36	0.27
Weighted sum of bin powers (wsum)	16.33	1.86
Square root(wsum)	4.15	0.47
Sorting of 22 envelope amplitudes	5.08	0.58
Loudness Growth Function (compression)	2.30	0.26
Conversion to electrical levels (M & T levels)	1.94	0.22
Total	48.78 (μ s)	5.56 (ms)

Table 1. Profiling outcome of the ACE implementation on the PDA. The numbers in the second column were obtained after averaging over 114 sub-frames.

2.3 Modifications to the SDIO board

In the previous quarterly report (QPR5), we described the development of the SDIO interface board. Following testing of the SDIO board, we found that several changes needed to be made to accommodate for sampling the microphone signal (acquired from the BTE unit rather than from the PDA) and inclusion of an external trigger signal for ECAP/EABR recording systems. Changes included: (a) addition of anti-aliasing filters for the A/D circuit, (b) addition of reset IC for AC2600 and reset switch for the FPGA, (c) addition of a sync output line from FPGA for triggering external EABR/ECAP recording systems, (d) addition of testpoints for debugging/monitoring data lines of AC2600, (e) addition of a 2-position jumper for enabling read/write protection for the EEPROM, and (f) addition of ESD Semtech diode protection of SDIO lines. The above changes to the board (now Version 2) have been submitted for fabrication.

2.4 Other activities

- We presented the following paper in CIAP'07 conference held in Lake Tahoe, CA:
Lobo, A., Loizou, P., Kehtarnavaz, N., Torlak, M., Lee, H., Sharma, A. Gilley, P., Peddigari, V. and Ramanna, L. (2007). "A portable research platform for cochlear implants," *Conference on Implantable Auditory Prostheses (CIAP)*, Lake Tahoe, CA, July 15-July 20.
- Submitted the following paper for publication:
V. Peddigari, N. Kehtarnavaz, P. Loizou, A. Lobo, P. Gilley and A. Sharma, "An interactive real-time cochlear implant research platform," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, October 2007.

2.4 Plans for next quarter

- Prepare documentation (User's and Programmer's guide) on the EEG data acquisition and post processing routines.
- Continue testing the SDIO interface board.
- Finish design of an 8-channel current stimulator with simultaneous stimulation capability.

Appendix

Lobo, A., Loizou, P., Kehtarnavaz, N., Torlak, M., Lee, H., Sharma, A. Gilley, P., Peddigari, V. and Ramanna, L. (2007). "A portable research platform for cochlear implants," *Conference on Implantable Auditory Prostheses (CIAP)*, Lake Tahoe, CA, July 15-July 20.

V. Peddigari, N. Kehtarnavaz, P. Loizou, A. Lobo, P. Gilley and A. Sharma, "An interactive real-time cochlear implant research platform," submitted to *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, October 2007.