Fifth Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Much effort was placed in this quarter on developing an interface board (see Section 2.2) to be used for interfacing and communicating with the Freedom (Cochlear Corporation) cochlear implant. We also worked on the design and testing of a single-channel stimulator (see Section 2.3) which can be used for chronic animal studies. Following the testing of the single-channel stimulator, we will focus on the design of a multi-channel stimulator with simultaneous stimulation capability. Finally, we continued our work on recording evoked potentials from scalp electrodes and implemented post-processing routines (see Section 2.1) for analyzing cortical auditory evoked potentials (CAEPs). This allowed online monitoring of recorded latencies without having to transfer the raw CAEP data to the PC for further processing.

2.1 Post-processing CAEP potentials

Work in this quarter involved the development of a post processing routine in LabVIEW to compute averaged (across multiple epochs) CAEP on the PDA. This allowed online monitoring of recorded latencies without having to transfer the raw CAEP data to the PC for further processing. The recordings were obtained from scalp electrodes using the CF-6004 compact flash card manufactured by National Instruments (NI). The task also involved designing a graphical user interface consisting of low pass filtering parameters and identifying the latencies of the computed evoked potentials. In addition, the issue of buffer overflow in the previously developed EEG recording routine was successfully resolved. The real-time EEG data acquisition routine was modified to support recordings for any number of epochs as opposed to a maximum of 250 epochs in the previous version.

A. CAEP recordings using LabVIEW

As described in Kim *et al*., (2007), a real-time data acquisition routine was developed in LabVIEW for collecting EEG data from human subjects on the PDA platform using the NI CF-6004 compact flash card. The recorded EEG data was stored in RAW data format for efficient utilization of the PDA limited memory resources. In order to extract CAEP, a post processing routine was written in LabVIEW which was optimized in terms of processing time by utilizing the hybrid programming approach described in Peddigari *et al*. (2007) based on C DLL's. The post processing routine allows one to analyze CAEP recordings interactively on the PDA platform and thus enables one to monitor the recorded latencies.

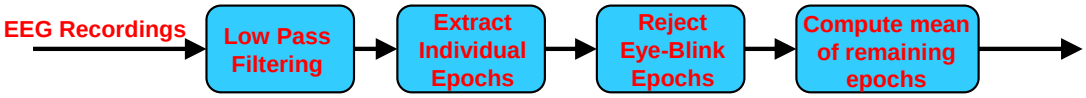


Figure 1. Overview of steps involved in evoked potential computation.

As illustrated in Figure 1, the computation of evoked potentials is carried out in two stages. In the first stage, the acquired recordings are passed through a low pass filter to remove the high frequency components of amplifier noise. Then, the data corresponding to each individual epoch along with eye blinks are extracted. This is achieved by finding the onset of a synchronization pulse and compensating for the delay between the start of the synchronization pulse and the playback of a stimuli speech signal over each epoch. More details on how this compensation delay is determined are given in Section 2.1.C. In the second stage, all the epochs having predominant eye blink activity are rejected and the remaining epochs are averaged to obtain the CAEP.

An interactive post processing program is used to compute the averaged evoked potential on the PDA. This was written using the LabVIEW PDA module utilizing the graphical programming approach, denoted by Version A in Figure 2. Since there was no hard real-time constraint for the above mentioned post processing program, it was decided to use off-the-shelf functional blocks for different modules such as filtering and reading of raw data files. The DAQmx RAW data utility functions were used for reading the EEG raw data files. The total post processing time required to compute the averaged evoked potential on the PDA was prohibitively large (more than 1 minute) as summarized in Table 1 for Version A. Thus, it was necessary to further optimize Version A utilizing the hybrid programming approach which involved using C DLL's for the time consuming modules. As indicated in Table 1, the module for reading the EEG raw data file containing recordings for 300 epochs took around 57 seconds using the DAQmx utility functions. Also, the low pass filtering module required another 11 seconds for filtering. The time required for the other modules (rejection of eye blink epochs and averaging) was found negligible compared to these modules.

As shown in Figure 3 (Version B), C DLL's were used to reduce the post processing time for reading the raw data files and for performing low pass filtering. The C DLL module for reading EEG raw data performed byte order reversal (little-endian to big-endian) on each of the 16-bit raw data integer sample read to avoid any loss in accuracy as the native host order on the PDA platform was big-endian. This module made use of the built-in functions supported by the Windows operating system. On the other hand, a fixed-point implementation was done for the low pass filtering since the PDA platform was powered by a fixed-point PXA 270 processor. The C code for the fixed point implementation of the low pass filtering using a cascade of second order sections was generated using the Fixed Point utilities available under the Digital Filter Design toolkit in LabVIEW. Using these optimized C DLL modules, the total post processing time for Version B was reduced to a total of less than 10 seconds, thus improving the computational efficiency of Version A.

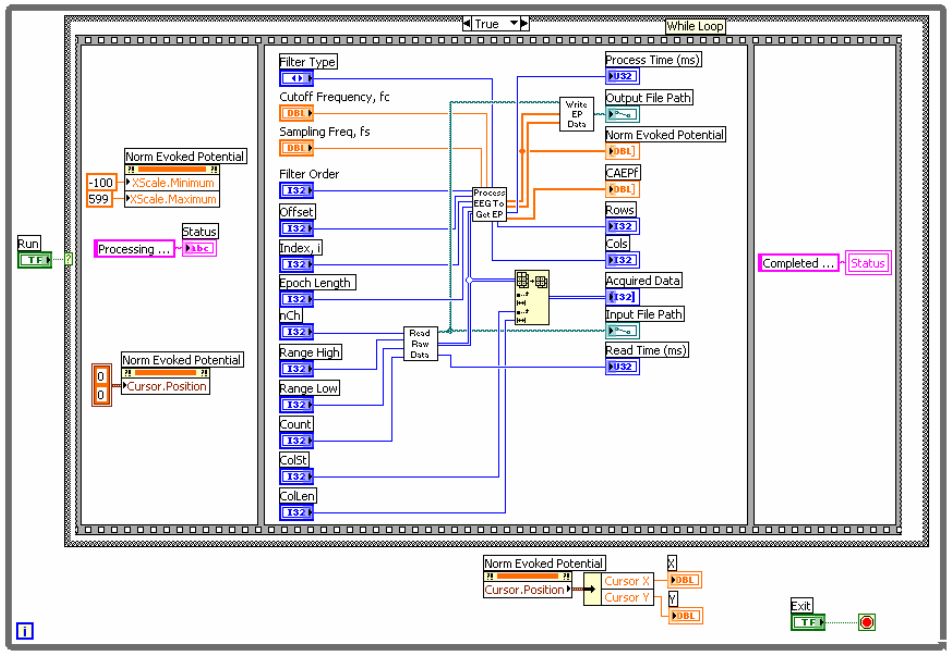


Figure 2. Earlier version (**Version A**) of the LabVIEW implementation for evoked potential computation using built-in functional blocks.

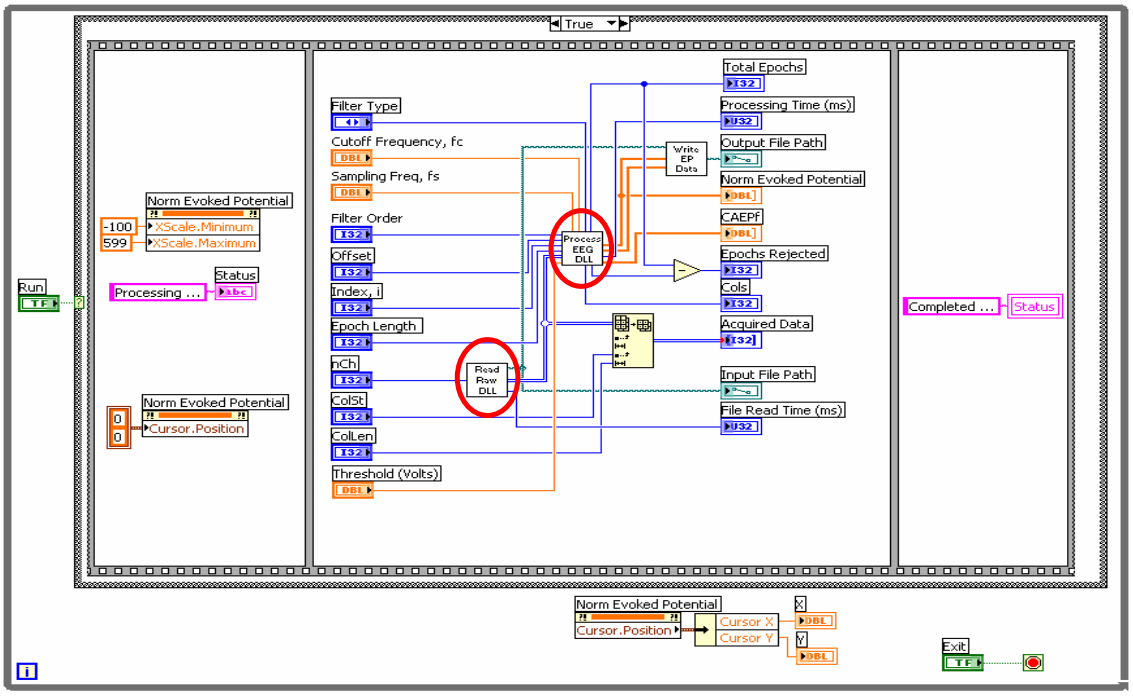


Figure 3. Optimized version (Version B) of the LabVIEW implementation for evoked potential computation (highlighted blocks denote C DLLs).

Sub-block or Component	Processing time (seconds) for EEG recordings data file with 300 epochs	
	Version A	Version B (A + DLL)
Reading RAW Data	56.7	5.4
Low Pass Filtering	10.6	3.4
Eye-Blink Rejection & Averaging	0.5	0.5
Total Processing Time	**67.8**	**9.3**

Table 1. Timing outcome corresponding to the various optimization steps.

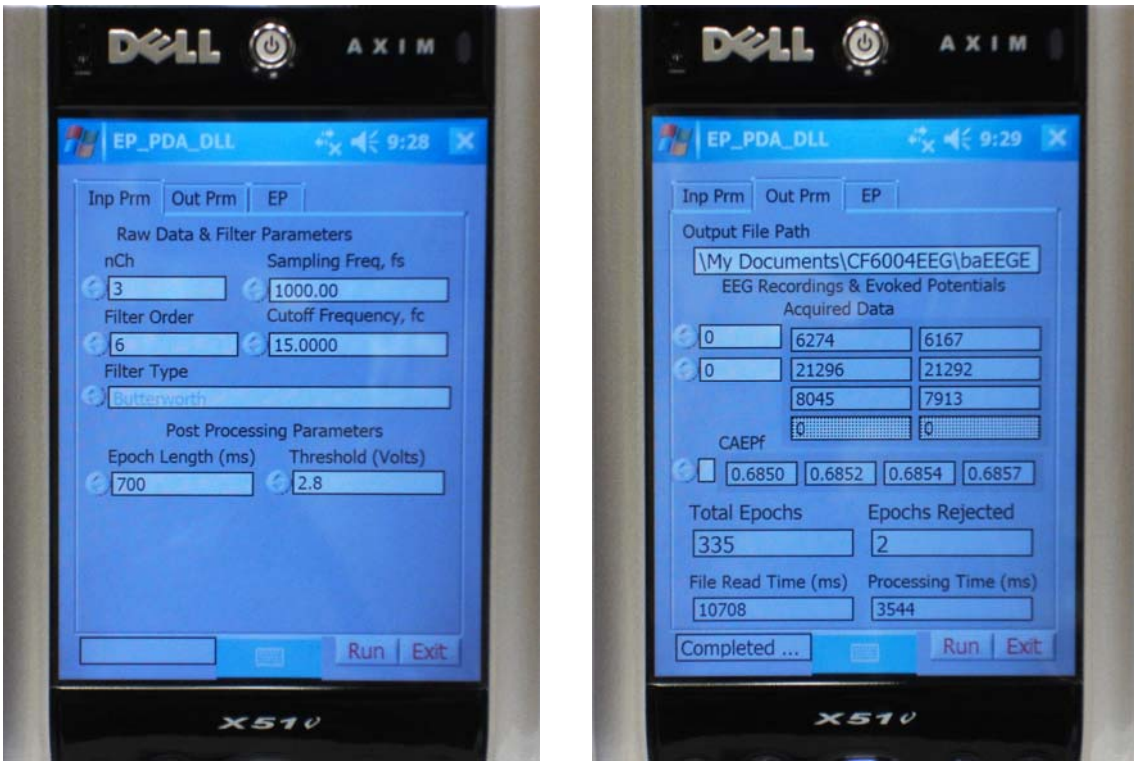
B. Interactive front panel for viewing and computing CAEP potentials and latencies

Both Version A and Version B provide an interactive front panel (see Figure 4) in the form of three panes using the TAB control supported by LabVIEW. The input parameters pane InpPrm shown in Figure 4 (a) allows users to vary the type, order and cutoff frequency of the low pass filter and the threshold (in volts) used to reject epochs with eye blinks. The output parameters pane OutPrm displays the number of epochs rejected, the timing spent for reading the raw data file, and the processing time for computation of evoked potentials, see Figure 4 (b). Finally, the evoked potential pane EP plots the evoked potential output for the selected data file and allows users to interactively find the latencies via indicators by moving the cursors over the waveform graph shown in Figure 4 (c).

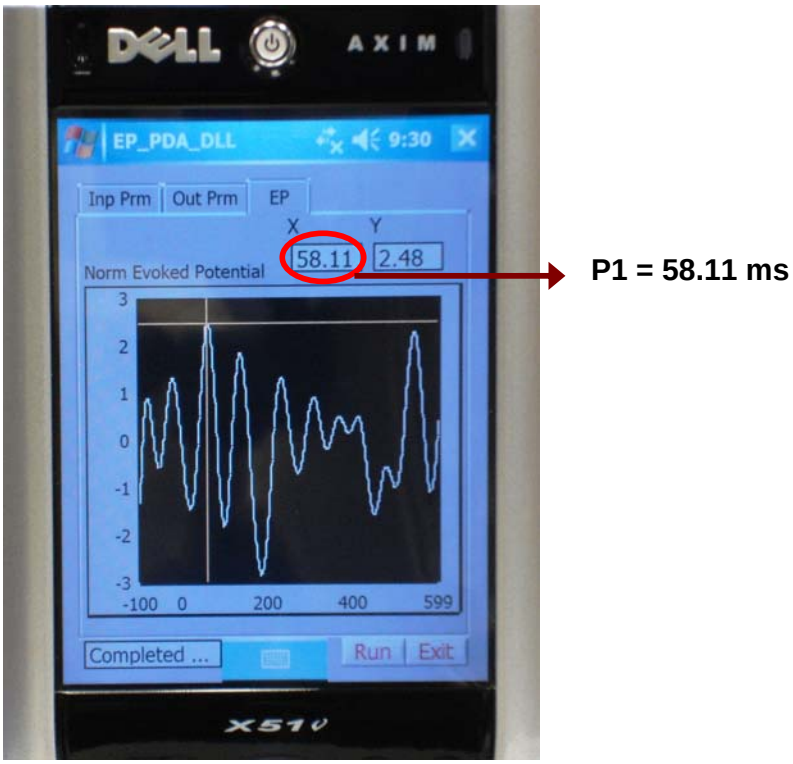
C. Compensation delay and buffer overflow issues resolved for NI CF-6004 Card

In order to determine the lag between the onset of the synchronization pulse and the recording of the EEG data for each epoch, a simple test was conducted using the oscilloscope and a real-time EEG data acquisition routine on the PDA platform. As discussed in Kim *et al*. (2007), the synchronization pulse was generated at one of the digital channels on the NI CF-6004 compact flash card and fed into one of its analog channels. The output of this analog channel along with the speaker output on the PDA platform was connected to an oscilloscope while running the real-time data acquisition program. Since the playback stimuli (speech signal) was known, the lag between the onset of the synchronization pulse and the start of the stimuli could be observed on the oscilloscope. This lag remained constant at 14 ms irrespective of the stimuli and current epoch. As a result, this delay of 14 ms was taken into account in the above mentioned post processing routine when computing evoked potentials.

Noting that the previously developed EEG data acquisition LabVIEW routine for the PDA platform did not allow recording the EEG data for a large of epochs (more than 250) due to buffer overflow, we investigated this issue further. The principal cause of the overflow was found to be the conversion of raw data into double precision after the data acquisition was halted. In the previous LabVIEW version of the EEG data acquisition routine, the recorded raw data were converted into double precision. The code segment converting all the epochs of the recorded raw data to double precision required more memory and hence this part was modified to convert only a portion of the raw data as selected by the user and to display it in a waveform graph in the front panel. This achieved a more efficient utilization of the available memory resources.



(a) Input parameters pane **(b) Output parameters pane**



(c) Evoked potential pane

Figure 4. Interactive GUI for evoked potential analysis n on the PDA. Hairline cross in panel (c) shows P1.

2.2 Interface board development

An interface board was developed for communicating and interfacing with the Freedom (Cochlear Corporation) cochlear implant. This board plugs into the Secure Digital Input Output (SDIO) slot of the PDA. The SDIO board enables the PDA to stimulate the Cochlear CI24 Freedom coil. Very briefly, the PDA sends stimulus amplitude packets to the SDIO card using the SDIO 4-bit communication protocol. The amplitudes are converted by the card to the Embedded protocol (Daly and McDermott, 1998) and finally stimulate the implant via the Freedom Coil. Figure 5 shows a schematic of the SDIO board.

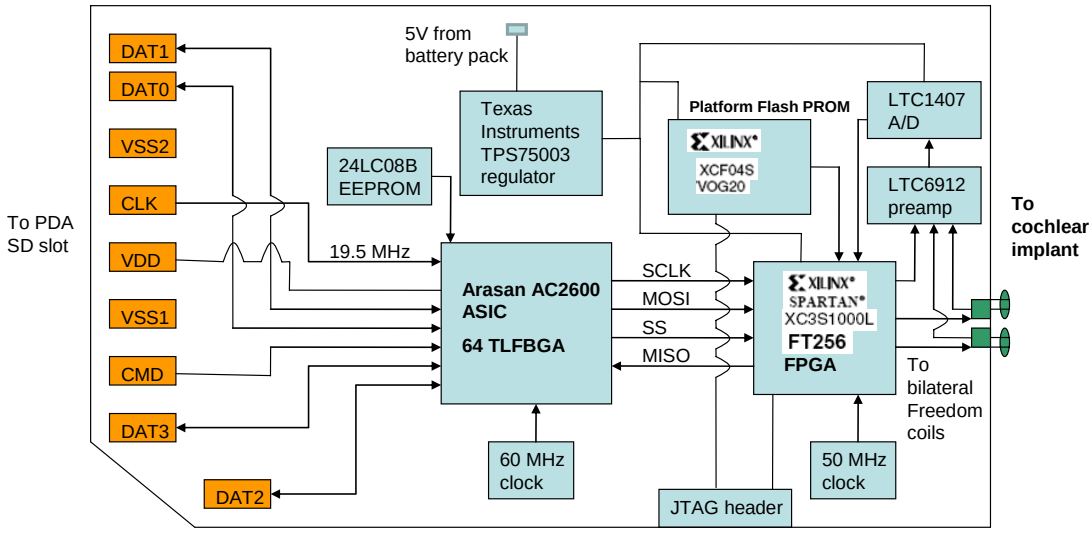


Fig. 5. Functional diagram of SDIO board.

The SDIO board consists of the following components:

Arasan AC2600 ASIC

The Arasan ASIC is a SDIO card controller and implements the SDIO standard 1.2 and SD Physical Layer specification 1.10. It communicates with the SDIO host controller on the PXA270 processor in the PDA via a command response interface. The ASIC converts the amplitude data into High Speed Synchronous Peripheral Interface (HSSPI) format and sends it to the FPGA. The ASIC is clocked by a 60 MHz crystal oscillator and generates a 30 MHz clock for HSSPI (SCLK). The ASIC also provides 8 and 16-bit processor interfaces for parallel data transfer.

24LC08B I2C EEPROM

The 24LC08B EEPROM stores the initialization parameters for the ASIC to startup in HSSPI mode. The EEPROM communicates with the ASIC via an I2C bus.

Xilinx XC3S1000L FPGA

The Xilinx FPGA receives the HSSPI amplitude packets from the ASIC and converts them to the Embedded protocol. The Embedded protocol bit stream is sent to the Freedom coil using a 5 MHz data signaling clock. The FPGA is clocked by a 50 MHz crystal. The FPGA logic implements a receive and transmit state machine and can support the 0.94 Mbps data link to the Freedom coil in the low rate stimulation mode using 5 cycles per cell Embedded protocol. The peak stimulation rate is 15,151

pulses/sec. Using 4 cycles per cell the peak stimulation rate becomes 19,608 pulses/sec. The SDIO board can be used for bilateral (or unilateral) cochlear implant studies. The left and right implants can be stimulated to within 0.2 microseconds of each other. The FPGA is also capable of stimulating the CI24 implant at the high rate mode of 32,000 pulses/sec. In addition, the CI22 implant can potentially be stimulated using the SEMA Expanded protocol with a 2.5 MHz data signaling clock.

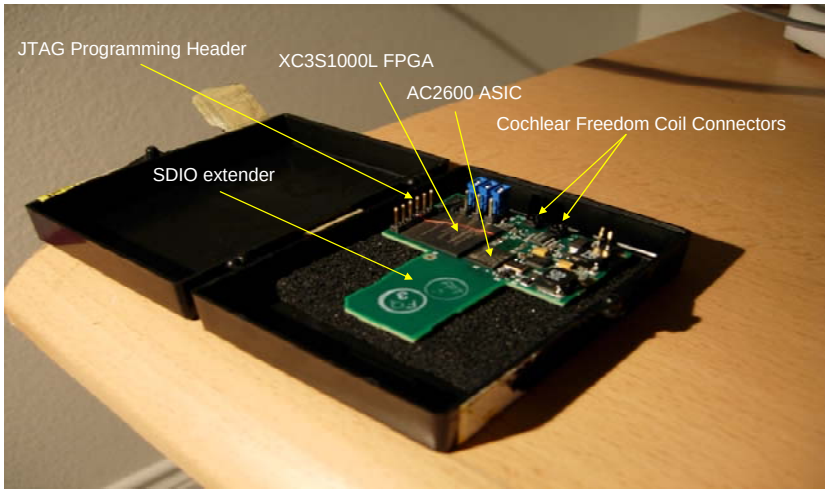
Xilinx XCF04S Platform Flash PROM
The Xilinx XCF04S is a Platform Flash PROM which stores the stimulation program logic from which the FPGA boots off during power on.

Linear Technology LTC6912 Preamplifier
The LTC6912 provides two independent inverting amplifiers with programmable gain. The LTC6912 is programmed by the FPGA over the Synchronous Peripheral Interface (SPI) bus.

Linear Technology LTC1407 A/D converter
The LTC1407 is a stereo A/D converter (ADC) and samples the microphone outputs from the bilateral BTE connected to their respective Freedom coils. The ADC has 1.5 Msps throughput per channel and presents a 14-bit two's complement digital output (interleaved left and right channels) to the FPGA. The samples are received by the FPGA over the SPI interface.

Texas Instruments TPS75003 Power Management IC
The TPS75003 is a triple-supply power management IC and supplies power to the FPGA and platform Flash PROM. The TPS75003 takes a 5 V input from the external battery pack and generates 1.2 V for VCCINT (core voltage), 3.3 V for VCCO (I/O voltage) and 2.5 V for VCCAUX (JTAG, Digital Clock Manager and other circuitry). The TPS75003 is a switching regulator (Pulse Width Modulation control) type and is "on" only when power is needed.

For the SPI interfaces above, the FPGA is the bus-master. The above SDIO board was fabricated (see Figure below) and is currently being tested.



2.3 Development of single-channel stimulator for animal studies

A chip was fabricated containing a new single-channel current stimulator implemented using AMS (Austriamicrosystems) 0.35 CMOS process. The single-channel current source consists of a newly designed current source, which can source or sink a 1mA output current with 9-bit current resolution. The new current source in the stimulator includes an output-impedance and voltage-compliance boosting scheme to preserve the accuracy of the output current even when the tissue impedance is highly variable.

Fig. 6 shows a picture of the chip of the single-channel current stimulator with JLCC 44 package. It should be noted that the area of the current stimulator only occupies part of the total chip area, which is 0.26mm^2.

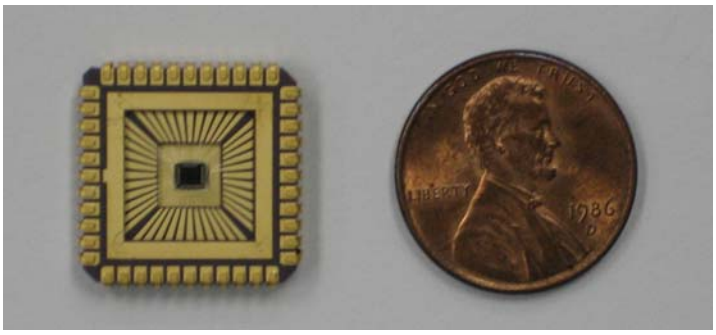


Fig. 6. Packaged single-channel current stimulator.

Fig. 7 shows the measured output current of the stimulator for different output voltages with input digital codes of 128, 256, 384, and 511. The current stimulator has a large voltage compliance of 4.77V (0.23V to 5V). The measured output impedance is at least 50MΩ for the output current of 1mA and output voltage ranging from 0.23 V to 5 V. These results verify that both wide voltage compliance and high output impedance are achieved simultaneously in the developed stimulator.

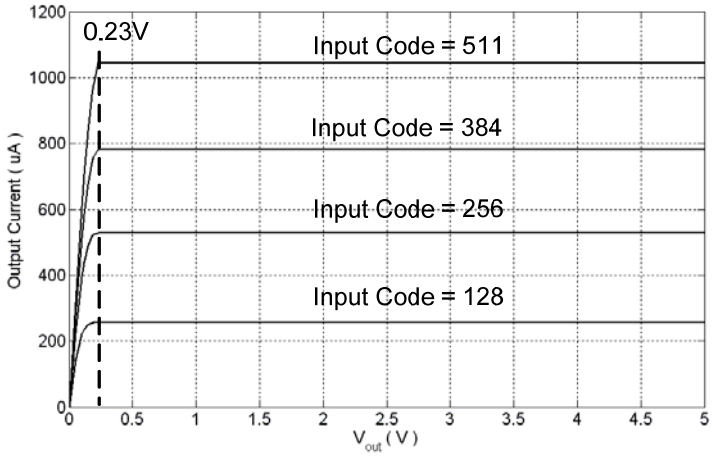


Fig. 7. Measured output current for different output voltages of the current source.

Fig. 8 shows the biphasic pulses generated by the single-channel current stimulator. The stimulator is controlled by a 2-bit digital input to determine sourcing or sinking output

current. The control signals (Fig. 8) can be used to produce arbitrary shape pulses. As shown in Fig. 8, the stimulator is sourcing or sinking 1mA output current with the pulse width set to 10μs and the stimulation rate set to 10,000 pulses/sec. The inter-phase gap is set to 8μs.

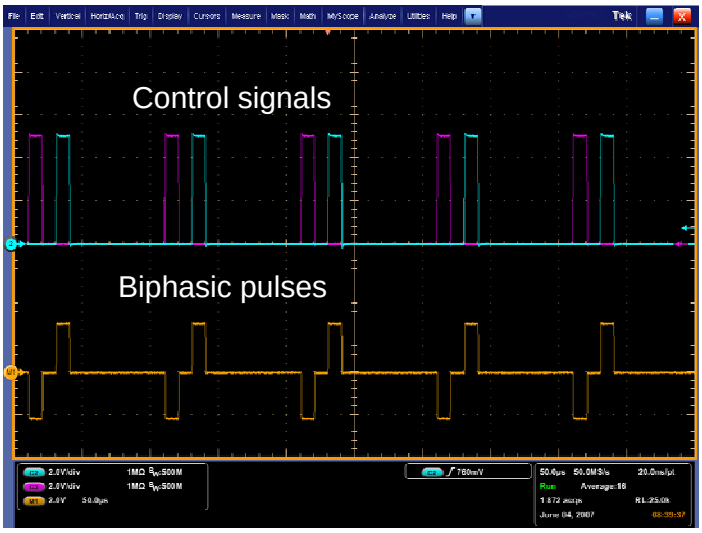


Fig. 8. Measured biphasic pulses of the single-channel current stimulator.

Table 2 provides the performance comparison between our developed current source in the stimulator with other state-of-the-art high-output-current designs. Our current source can deliver the largest output current, has the highest amplitude resolution, widest voltage compliance and largest output impedance, while maintaining a small implementation area.

	Ghovanloo &. Najafi (2005)	DeMarco *et al.*, (2003)	***Our work***
Supply voltage (V)	5	±5.5	***5***
Maximum Output Current (mA)	0.21	0.4	***1***
Resolution	5 bits	8 bits	***9 bits***
Maximum INL (LSB)	N.A.	-3.11	***2.9***
Maximum DNL (LSB)	N.A.	2.15	***0.8***
Voltage Compliance (V)	4.25	N.A.	***4.77***
Output Impedance (MΩ)	18.8	0.443	***>50***
Area (mm^2)	0.05	0.227	***0.26***

Table 2. Performance comparison with previously reported current sources.

2.4 Plans for next quarter

- Submit a journal paper summarizing our work thus far to *Acta Acustica United with Acustica*. Paper is tentatively entitled: "An Interactive Real-Time PC and PDA-Based Cochlear Implant Research Platform".

- Prepare documentation (User's guide) on the EEG data acquisition and post processing routines.
- Continue testing the SDIO interface board.
- Present the following paper in CIAP'07 conference to be held in Lake Tahoe, CA:
  Lobo, A., Loizou, P., Kehtarnavaz, N., Torlak, M., Lee, H., Sharma, A. Gilley, P., Peddigari, V. and Ramanna, L. (2007). "A portable research platform for cochlear implants," to appear in C*onference on Implantable Auditory Prostheses (CIAP)*, Lake Tahoe, CA, July 15-July 20.
- Based on our current single-channel current stimulator, we will continue to design an 8-channel current stimulator with simultaneous stimulation capability. Additionally, our work on single-channel current stimulator will be submitted for publication in the *IEEE International Symposium on Circuits and Systems* conference.

References

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