Fourth Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Much effort was placed in this quarter on recordings of cortical auditory evoked potentials (CAEPs) using two different data acquisition cards. A signal-preconditioning circuit was required for one of two cards, and we report on the development of an interface board with the appropriate conditioning circuitry. CAEP recordings were made successfully on the PDA using the two data acquisition cards programmed in C and LabVIEW environments. The CAEP data were analyzed and compared. Finally, we report on improvements made to the LabVIEW real-time implementation of the noise-band vocoding algorithm on the PDA.

2.1 Interface board for EEG data acquisition on the PDA

In Loizou et al. (2006), we reported on EEG data acquisition on the PDA using the C-Cubed Dataq-CF2™[1] compact flash card that plugged into the PDA. The Dataq-CF2™ card was connected to the Grass Technologies[2] P511K pre-amplifiers and required some amount of signal pre-conditioning to obtain good recordings. To further improve the accuracy and reliability of the data acquisition on the Dataq-CF2™ compact flash card, we focused on the development of an interface board between the Dataq-CF2™ compact flash card and the Grass pre-amplifiers.

This board, henceforth called EEGB-02, serves as an interface between the amplified EEG signals generated by the Grass pre-amplifiers and the Dataq-CF2™ card. The output of the Grass P511K, must undergo additional conditioning in order to meet the input signal requirements of the Dataq-CF2™ card for accurate and reliable acquisition. This includes high pass filtering, the addition of a +1.25 VDC offset, and voltage amplification. A block diagram of the EEGB-02 signal conditioning circuit (at a high level) is shown in Fig. 1.

[1] C-Cubed Ltd. www.c-cubed.co.uk
[2] Grass Technologies. http://www.grasstechnologies.com

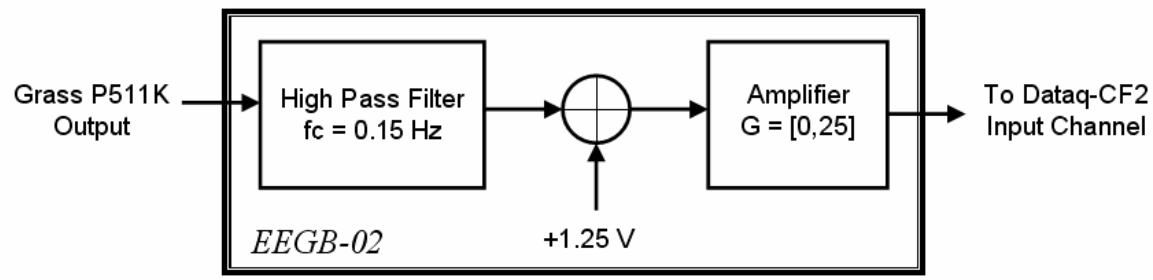

Figure 1. Functional block diagram of the EEGB-02 interface board.

The single-ended EEG output signal of the Grass P511K is wired into the input channel of the EEGB-02 where it is first filtered by a Bessel high pass filter with cut-off frequency fc = 0.15 Hz. Ideally, the EEG signal is to be positioned in the center of the Dataq-CF2 dynamic input voltage range, Vcenter = +1.25 V, in order to utilize the full resolution of Dataq-CF2's digital-to-analog converter. But often times the EEG signal is off-centered by some arbitrary DC voltage other than +1.25 V. The Bessel high pass filter eliminates this arbitrary DC offset; and the following stage, the voltage adder, centers it about the middle of the Dataq-CF2's dynamic input voltage range. The EEG signal is then amplified once more such that it fills the dynamic input voltage range of the Dataq-CF2 as fully as possible. The outputs of the EEGB-02 are then forwarded to the input channels of the Dataq-CF2 for sampling. A detailed description of the EEGB-02 board and the circuit implementation of the various signal conditioning functions are provided in the following sections.

2.1.1 Specifications

The EEG interface board has the following features:

- Four isolated EEG channels with independent power supplies and reference planes
- Four single-ended input channels and four single-ended output channels
- Dynamic range in gain: 0 - 25
- Nominal output voltage range: 0 – 2.5 V
- Input Supply Voltage: +5 VDC

The following table summarizes the electrical characteristics of the board:

PARAMETERS	MIN	TYPICAL	MAX	UNITS
Supply Voltage	4.5	5	5.5	V
Input Signal Voltage	-11.25		13.75	V

2.1.2 Design Description

The following is a description of the six major sections of the EEGB circuit board: High-pass filter, +1.25 V DC Offset Addition, Inverting Amplifier, Offset Reference Voltage Circuits, and Power Supply Circuits.

2.1.2.1 High-pass filter

The first stage of the EEG channel is a high pass filter that attenuates signals with frequencies less than 0.15 Hz. Because the output of the Grass P511K may have some arbitrary DC offset value which is of no interest, the high pass filter eliminates the offset and centers the EEG signal around 0 V while preserving the information bearing signals embedded in the higher frequencies. The high pass filter is a two stage, four pole Bessel filter with unity gain in the pass band (shown in Fig. 2) and was designed using the Texas Instrument[3] Filter Pro (v. 2) filter design software tool.

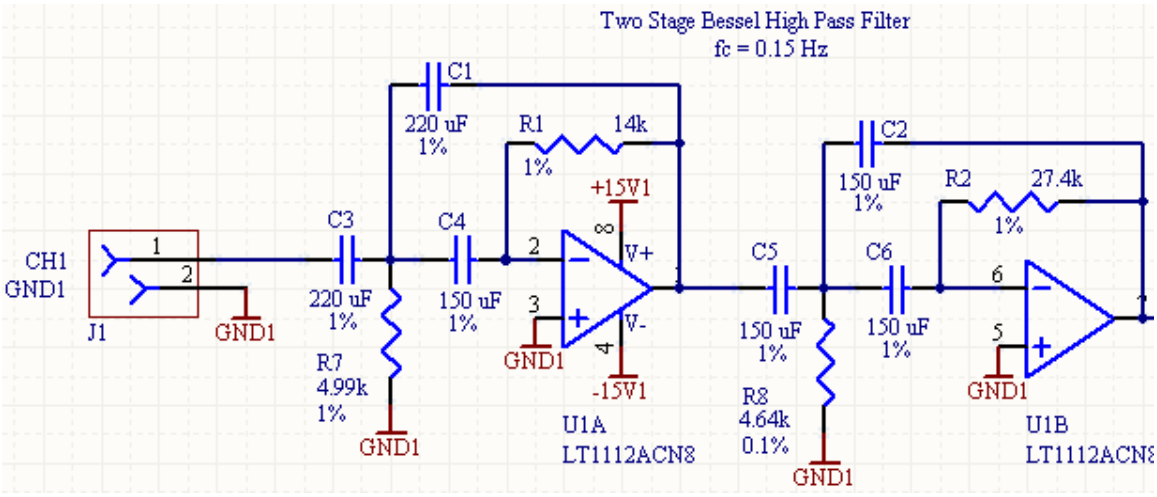

Figure 2. Two stage Bessel high pass filter circuit.

2.1.2.2 DC Offset Addition

The second stage of the EEG channel is an inverting adder which offsets the filtered output in stage 1 by +1.25 V. Because the Dataq-CF2™ Compact Flash Data Acquisition module requires input signals to be within the voltage range of 0 to +2.5 V, the AC output of stage 1 (centered around 0 V) is offset to the center of the required input voltage range of the Dataq-CF2™, +1.25 V. The inverting adder circuit is shown in Fig. 3.

[3]Texas Instruments. http://focus.ti.com/docs/toolsw/folders/print/filterpro.html

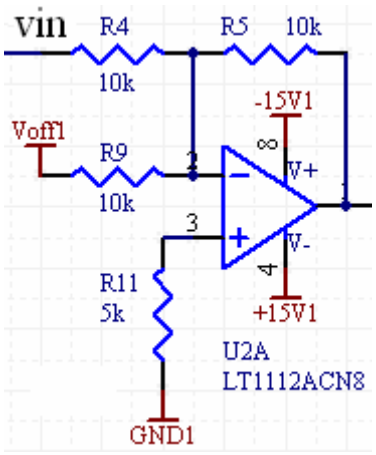

Figure 3. Inverting adder circuit with unity gain.

Voltage offset of the input signal, vin, to the left of resistor R4 is performed according to the following equation.

$$vout = -\left(vin\frac{R_5}{R_4} + v_{off1}\frac{R_5}{R_9} \right) \qquad \text{Eq. 1}$$

where Voff1 = +1.25 V and R4 = R5 = R9 = 10 kΩ, reducing Eq. 1 to

$$vout = -\,(\,vin + 1.25\,). \qquad \text{Eq. 2}$$

Note that the output of the amplifier is the *inverted* sum of the input signal, vin, and the DC offset of +1.25 V. Because of this inversion, the output signal must be inverted once more before it can be sampled by the Dataq-CF2™, and is done so in the upcoming stage.

2.1.2.3 Inverting Amplifier

The inverted output signal of stage 2 must be inverted once more before it is ready to be sampled by the Dataq-CF2™. This inversion is performed by the inverting amplifier shown in Fig. 4.

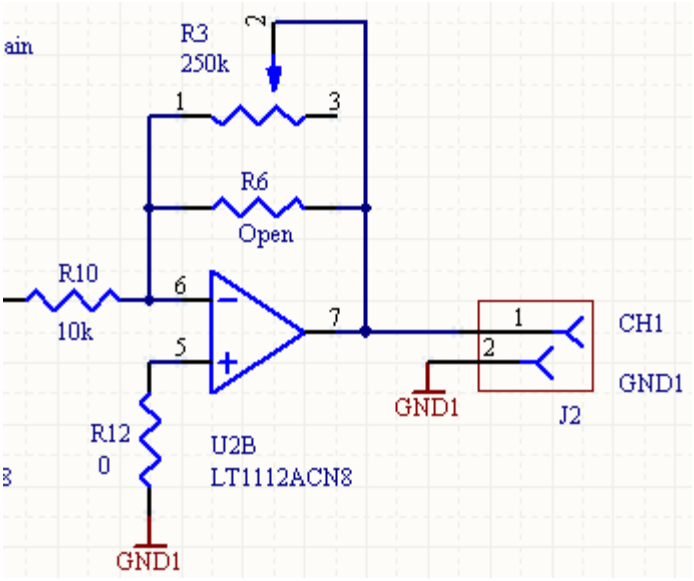

Figure 4. Inverting amplifier with unity gain.

The output of the inverting amplifier, vout, is related to the input, vin, by the following equation.

$$vout = - vin * R3 / R10. \quad \text{Eq. 3}$$

The gain of the amplifier is the negative ratio of resistor R3 to potentiometer R10,

$$G = - R3 / R10 \quad \text{Eq. 4}$$

where R10 = 10 kΩ and potentiometer R3 ranges from 0 to 250 kΩ, yielding a dynamic range in gain of 0 to -25:

$$0 \leq | G | \leq 25. \quad \text{Eq. 5}$$

Thus, with the appropriate selection in gain, the output of the inverting amplifier is the amplified EEG signal which fits within the voltage range of the Dataq-CF2™ Compact Flash data acquisition module – ready for analog-to-digital sampling.

2.1.2.3 Offset Reference Voltage

As mentioned above in the description of the inverting adder, the filtered output of the high pass filter in stage 1 is offset in voltage by a +1.25 VDC source. This reference voltage is generated by the TPS79601 low-dropout linear regulator made by Texas Instruments[4]. The +1.25 V offset reference voltage circuit is shown in Fig. 5.

[4] Texas Instruments. www.ti.com

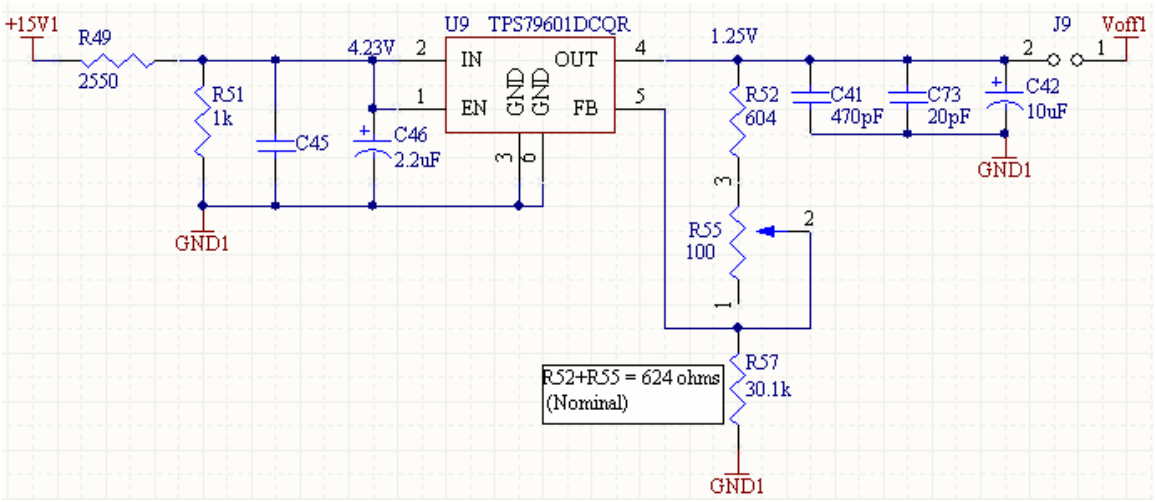

Figure 5. Offset voltage reference circuit.

Because the TPS79601 (U9) has a limited input power supply range of 2.7 to 5.5 V, the +15 V source to the left at R49 is reduced to 4.23 V at U9-2 by the voltage divider comprised of R49 and R51.

The output voltage, vout, of the TPS79601, U9-4, is adjustable according to the following equation.

$$vout = 1.2246 * [\ 1 + (\ R52 + R55\ ) / R57\ ] \qquad \text{Eq. 6}$$

where R52 = 604 Ω, R57 = 30.1 kΩ, and R55 is a 100 Ω trim-pot. Thus, for a desired output voltage of 1.25 V, the series resistance of R52 and R55 must be equal to 624 Ω or

$$\mathbf{R55 = 20\ \Omega}. \qquad \text{Eq. 7}$$

Note that the adjustment of trim-pot R34 should be performed with jumper J9 removed. The voltage offset, Voff1, should be tuned to 1.25 V before it is applied to any other loads which could potentially be damaged by any voltage greater than 1.25 V.

The capacitance, C41, at the voltage output, U9-4, was calculated using the following formula:

$$C_{41} = 3\times10^{-7}\left(\frac{R_{52}+R_{55}+R_{57}}{R_{57}(R_{52}+R_{55})}\right) \qquad \text{Eq. 8}$$

Substituting the values for R52, R55, and R57 used in calculating Eq. 7 back into Eq. 8 yields C41 = 490 pF. However, since capacitors are only available in discrete values, 490

pF not being one of them, C41 is chosen to be 470 pF and placed in parallel with another 20 pF capacitor, C73, for an equivalent capacitance of 490 pF.

2.1.2.4 Power Supply Circuits

The Texas Instrument[5] DCP010515 dual output DC/DC converters supply the LT1112 high precision op-amps with ±15 V as shown in Fig. 6.

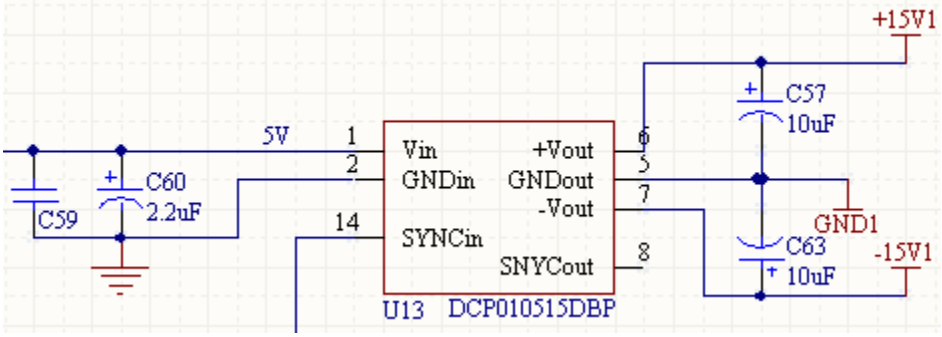

Figure 6. Dual Output ±15 V Circuit.

The DCP010515 converts the 5 V supply voltage, U13-1, to +15 V, U13-6, and -15 V, U13-7. To minimize coupling at the input and rippling at the output, capacitors with low equivalent series resistance (ESR) should be used. The four EEG channels of the EEGB are isolated in order to minimize interference between adjacent channels. Because of the isolation requirement, a single DCP010515 is used to power each EEG channel – each with its own +15 V, -15 V, and GND plane. These planes are not shared among the four individual EEG channels, but are separate and isolated.

The SYNCin port of the DCP010515, U13-14, serves to eliminate beat frequencies and other electrical interference which arise as a result of the small variations in switching frequencies among the four DCP010515's. This is overcome by synchronizing the four DCP010515's by connecting their SYNCin ports together with jumpers J13, J14, J15, and J16 (not shown in Fig. 6).

The first prototype of the EEGB-02 board has been manufactured and tested (see details in the next section). Figure 7 shows a snapshot of first version of the prototype board. Supporting documentation such as the design description and test procedure for the board are available. Test results revealed only minor issue with the design which will be corrected in the next revision of the board.

[5] Texas Instruments. www.ti.com

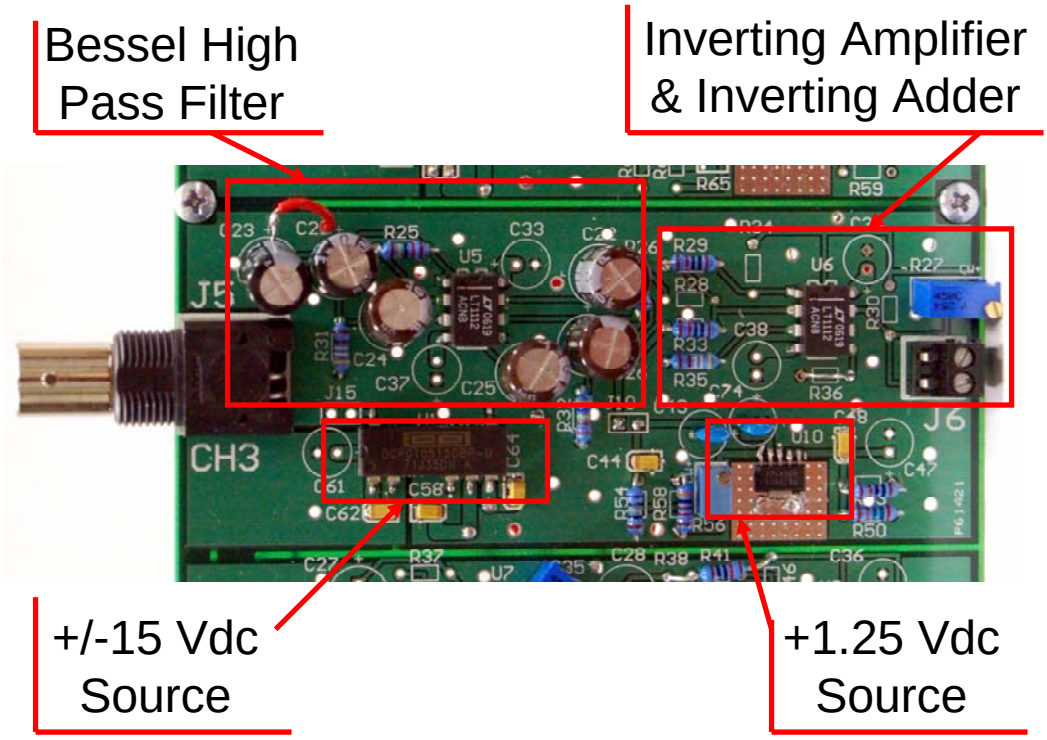

Figure 7. The manufactured EEGB-02 interface board.

The Tables below gives a description of the input/output connectors and jumpers of the EEGB-02 board.

CONNECTOR	DESCRIPTION
J1	Channel 1 input
J2	Channel 1 output
J3	Channel 2 input
J4	Channel 2 output
J5	Channel 3 input
J6	Channel 3 output
J7	Channel 4 input
J8	Channel 4 output
P1	+5 VDC power supply

JUMPER	DESCRIPTION
J9	Channel 1 Voff1 calibration. Remove during calibration.
J10	Channel 2 Voff2 calibration. Remove during calibration.
J11	Channel 3 Voff3 calibration. Remove during calibration.
J12	Channel 4 Voff4 calibration. Remove during calibration.
J13	Channel 1 ±15 V supply SYNCin. Install to synchronize supplies.
J14	Channel 2 ±15 V supply SYNCin. Install to synchronize supplies.
J15	Channel 3 ±15 V supply SYNCin. Install to synchronize supplies.
J16	Channel 4 ±15 V supply SYNCin. Install to synchronize supplies.

The above board was used and tested with the C-Cubed Dataq-CF2 card for EEG data acquisition. Details of the testing and evaluation are given next.

2.2 CAEP recordings on the PDA using two different data acquisition cards

Cortical auditory evoked potential (CAEP) recordings were obtained on the PDA using two different A/D cards. Each A/D card was programmed using a different custom stimulation program. The first card (C-Cubed Dataq-CF2™) was programmed in C (details were provided in previous technical report – Loizou *et al*., 2006) and the second card (CF-6004, National Instruments) was programmed using LabVIEW.

An interactive real-time data acquisition program (see Figure 8) was written using the LabVIEW PDA module and the LabVIEW DAQmx utility for the NI CF-6004 compact flash card. The program provides an interactive GUI for the user to configure both the analog and digital channels of the CF-6004 card for data acquisition, synchronization pulse generation and buffer size allocation. It enables the user to select the stimuli and various parameters, such as inter stimulus interval and number of epochs the stimuli to be repeated, during data acquisition. In addition, it provides options for storing the acquired data and displaying any required portion in an interactive manner. As shown in Figure 9, the real-time data acquisition routine developed in LabVIEW consists of initiating acquisition, generating a sync pulse to indicate the onset of the stimuli playback, playing the stimuli and then writing the acquired EEG data into a buffer. The above process repeats within a real-time loop through an interactive GUI. Some of the major issues that needed to be resolved included the generation of the synchronization pulse and the storage of the acquired data based on the limited available memory. The latter issue was resolved by acquiring the EEG data in raw format as 16-bit integers and storing them in binary format. The synchronization of the recordings with stimulus playback is described next.

As described in Lobo et al. (2006), the CF-6004 card[6] has four analog channels and four programmable digital i/o channels. Of the 4 analog channels, one was used to record the EEG signal and another to record the eye blink activity. One of the remaining two analog channels was connected to one of the digital channels. A synchronization pulse using read and write VIs was generated and placed on that digital channel. To avoid any jitter during stimuli playback, a programmable delay of 100 ms was inserted between the pulse generation and the playback. Hence, the actual EEG activity and playback were started after 100 ms delay from the onset of the synchronization pulse during each repetition of the stimuli playback.

[6] National Instruments, *NI CF-6004 Compact Flash Data Acquisition for PDAs*, http://sine.ni.com/nips/cds/view/p/lang/en/nid/201664

Figure 8. Interactive GUI of real-time EEG data acquisition program.

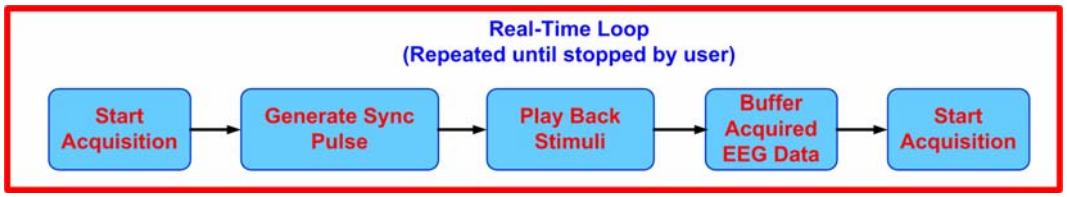

Figure 9. Real-time EEG data acquisition implementation.

Continuous electroencephalographic activity (EEG) was acquired from a normal-hearing adult subject while listening in a sound-attenuating booth to the speech syllable "ba" presented at about 70 dB SPL in sound-field. The EEG was recorded from the Cz electrode referenced to the right mastoid. A separate bipolar channel was used to monitor eye blinks. The stimulus was presented approximately 300 times for each recording. Analog EEG was captured from two Grass amplifiers with an analog, band-pass filter setting of 1-100 Hz at a gain of 1000.

Following the recordings, the EEG was divided in to epochs with time zero set to the onset of the speech stimulus. Epochs containing eye blinks were rejected from further analysis. After eye blink rejection, the remaining epochs were baseline corrected to the

average amplitude for each epoch, and then averaged to produce a cortical auditory evoked potential (CAEP).

Results of the CAEPs from each A/D card are shown in Figure 10. The peaks of the CAEP – the P1, N1, and P2 – are labeled with arrows for each of the CAEP responses. Note that there is a difference of approximately 17 ms between peaks from the two A/D cards. This difference is of interest, because it may be an indicator of a sync pulse delay or offset in one, or both of the PDAs sending the auditory stimulus. That is, the actual time at which the auditory stimulus is presented from the soundfield speaker may be slightly different from the actual time that the sync pulse is recorded in the A/D sync channel. Another scenario might be that the delay is not in the sync pulse, but instead in the time delay between the actual occurrence of the EEG activity and the sampling from the A/D conversion. As a note, the inter-stimulus intervals between stimuli from the PDA equipped with the C-cubed A/D card were notably more variable (i.e., more temporal jitter) than the PDA equipped with the National Instruments card. The stimulus jitter from the C-cubed PDA may have contributed to the latency differences between the two cards. As anecdotal support for this, the known P1 latencies for this subject are typically closer to those seen from the NI card.

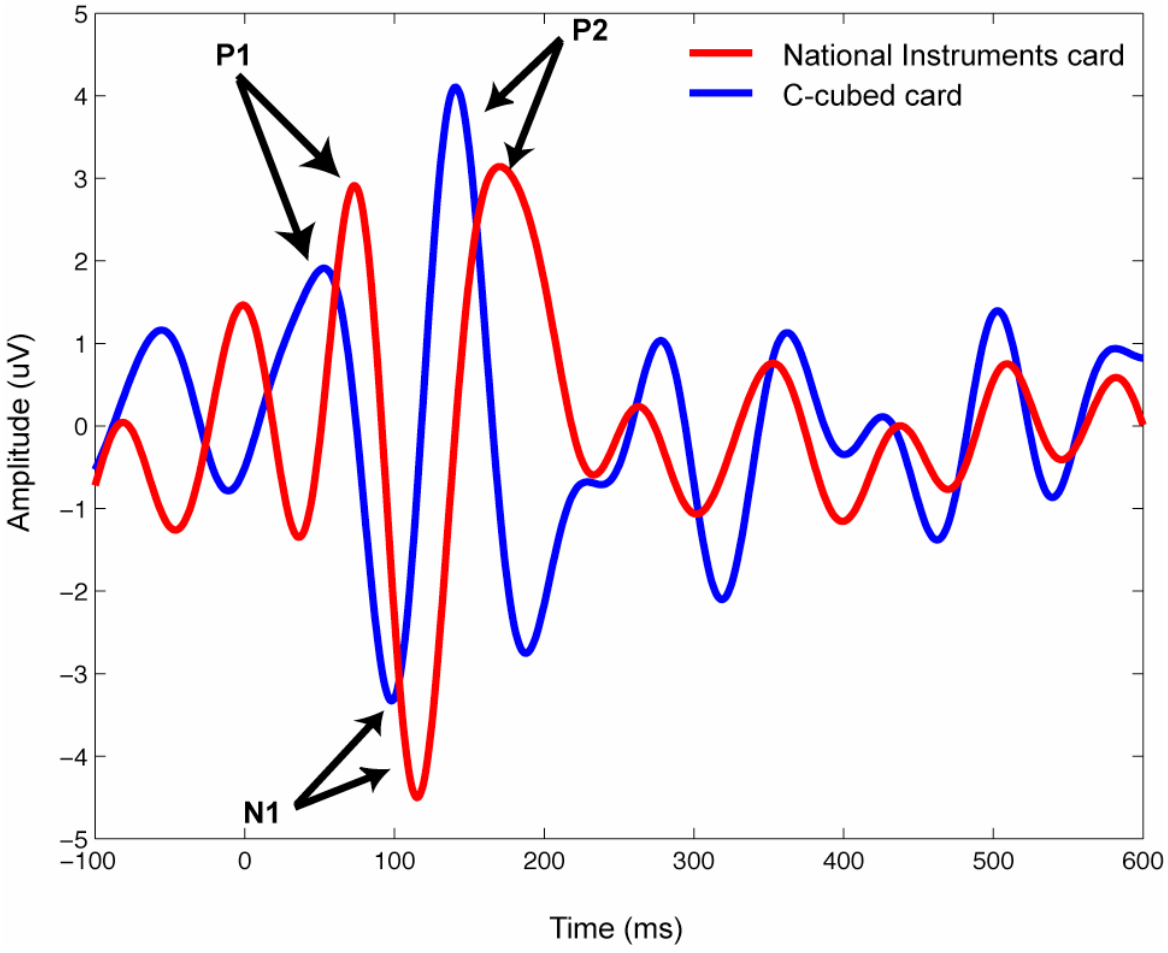

Figure 10. CAEPs recorded on the PDA using two different data acquisition cards. These recordings were made in response to the syllable "ba".

In summary, we recorded CAEPs from a single normal-hearing subject using two different A/D cards programmed on two different PDAs. Overall, the morphology of the CAEPs was similar between the two cards, suggesting that the A/D cards are adequately capable of acquiring EEG data. However, slight variation in the peak latencies of interest suggest that some tweaking of the stimulation sync pulse and the acquired EEG is necessary, and this will be investigated in the next quarter.

2.3 Improving the LabVIEW real-time implementation of the noise-band vocoder on the PDA

The real-time LabVIEW implementation of the signal processing components on the PDA platform was redesigned based on Windows APIs in order to acquire input signal frames and subsequently play back the synthesized frames. This was achieved via hybrid programming in LabVIEW (Kehtarnavaz and Peddigari, 2007) by calling the Windows APIs through the Dynamic Link Libraries (DLLs) written in C. The key advantage of this improvement was to allow acquisition of smaller frame lengths as low as 512 samples, compared to 2205 samples in the earlier implementation (Loizou *et al*., 2006). The use of smaller frame lengths reduces the lag between two consecutive frames and thus enhances the real-time performance when playing back the synthesized frames.

The implementation of acquiring input frames and playing back the synthesized frames was achieved using the CALLBACK function options supported by Windows APIs. The design stage involved the computation of the filter coefficients and other parameters in an interactive way through the PDA GUI illustrated in Figure 11. Upon the initiation of the vocoder signal processing, the designed parameters were passed via a C DLL to initialize the global parameters declared within the C DLL. These initialized global parameters, such as filter coefficients, frame length, were then utilized within a real-time loop. It should be noted that the real-time loop was implemented via the CALLBACK function wherein each acquired frame was processed using the stored global parameters. To allow for efficient use of memory, the appropriate resources were de-allocated once the vocoder signal processing was stopped by the user.

A thorough analysis and study was carried out to examine the impact of the fixed-point arithmetic computation on the accuracy of the noise-band vocoder implementation (Loizou, 2006). As PDA platforms are normally powered by fixed-point processors, the floating-point filter coefficients generated during the design stage were converted to fixed-point via scaling. We observed that although Q14 format was adequate for pre-emphasis and low pass filtering, Q20 format was required for the band pass filtering to minimize any loss in numerical accuracy. Note that the input samples were 16 bit integers and a 64-bit accumulator was thus utilized for the computation of the low pass and band pass filter difference equations.

Figure 11. Interactive GUI of LabVIEW implementation of noise-band vocoder.

Utilizing Windows APIs not only allowed us to decrease the delay between two consecutive frames being played back via smaller frame lengths but also helped us to reduce the processing time for each frame (see Table 1). In the previous implementation (Loizou et al., 2006; Peddigari et al. 2007), frames were acquired in the LabVIEW environment and then passed to C DLLs to synthesize speech. We noted that there was an overhead associated with passing the data in and out of the C DLLs for the acquired frames. Since the enhanced implementation acquires input frames using Windows APIs within the C DLLs, the overhead is considerably reduced, leading to a reduction in the total processing time. As shown in Table 1, the total processing time for a frame length of 46.4 ms takes on the average only 16 ms. That is, Version E processing time is less than $1/3^{rd}$ of the frame length. On the other hand, the previous implementation required 77 ms to obtain synthesized frames for a 100 ms input frame length (Loizou et al., 2006). That is, the total processing time was around $3/4^{th}$ of the frame length for Version D. Thus, with the above mentioned modifications we have successfully improved the real-time performance and the fixed-point aspect of the LabVIEW implementation on the PDA platform.

Sub-block or Component	Processing time for 100 ms frames (ms)				46.4 ms frames (ms)
	Version A	Version B (A + DLL)	Version C (B + MA)	Real-Time Version D (C + FPA)	Improved Real-Time Version E
DC Offset Removal	7	5	3	*1*	**0.1**
Pre-Emphasis	11	8	5	*3*	**0.4**
Bandpass Filtering (Decomposition & Synthesis)	1450	705	412	*34*	**12**
Full Wave Rectification	40	23	15	*7*	**0.5**
Lowpass Filtering	260	135	76	*24*	**2**
White Noise Excitation	60	32	19	*8*	**1**
Total Processing Time	1828	908	530	*77*	**16**

Table 1. Timing outcome corresponding to the various optimization steps. For description of the different implementation versions (A-D), see Loizou et al., (2006).

2.4 Plans for next quarter

- We will continue with the implementation of other signal processing algorithms on the PDA. More specifically, we will pursue the implementation of the ACE strategy used by Cochlear Corporation in their Nucleus-24/Freedom device.
- For the CAEP data acquisition on the PDA, we are planning to resolve the latency differences between the two data acquisition cards.
- We will continue with the development of an interface card (via the SD slot of the PDA) that would communicate with the coil or BTE unit of commercial implant devices.
- Test manufactured single-channel current source.
- Present the following two accepted papers in conferences:
    1. V. Peddigari, N. Kehtarnavaz and P. Loizou, "Real-time LabVIEW implementation of cochlear implant signal processing on PDA platforms," to appear in *Proceedings of IEEE International Conference on Signal, Acoustics and Speech Processing,* Hawaii, April 2007.
    2. Lobo, A., Loizou, P., Kehtarnavaz, N., Torlak, M., Lee, H., Sharma, A. Gilley, P., Peddigari, V. and Ramanna, L. (2007). "A PDA-based research platform for cochlear implants," to appear in *3rd International EMBS Conference on Neuroengineering*, Hawaii, May 2007.

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