Eleventh Quarterly Progress Report

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Open Architecture Research Interface for Cochlear Implants

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1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Work in this quarter focused on describing the changes made to the latest revision (v.3) of the SDIO interface board. All hardware components of the v.3 board have been successfully tested and debugged. The SDIO board has also been tested using a Verizon XV6800 mobile phone running on Windows' Mobile 6.0 operating system. Finally, we report on the integration of the LabVIEW code with the SDIO interface board. This provides the additional flexibility to the researcher to develop and investigate new speech-processing algorithms in C or LabVIEW.

2.1 Hardware testing of SDIO board (v. 3)

The latest revision of the SDIO interface board (v.3) incorporates an overall reduction in size by eliminating unnecessary components such as test points, jumpers, and LEDs that were used in the early stages of developing and debugging the prototype version of the board. The digital-to-analog (DAC) circuitry from v.2 was also removed as it too was no longer needed. As a result, a 24% reduction in overall board size was achieved.

The surface area of the SDIO interface board (v.2) was reduced from 4.025 in^2 to an overall surface area of 3.065 in^2 with the latest board (v.3). The difference in size is apparent when then two boards are place beside each other as shown in Fig. 1.
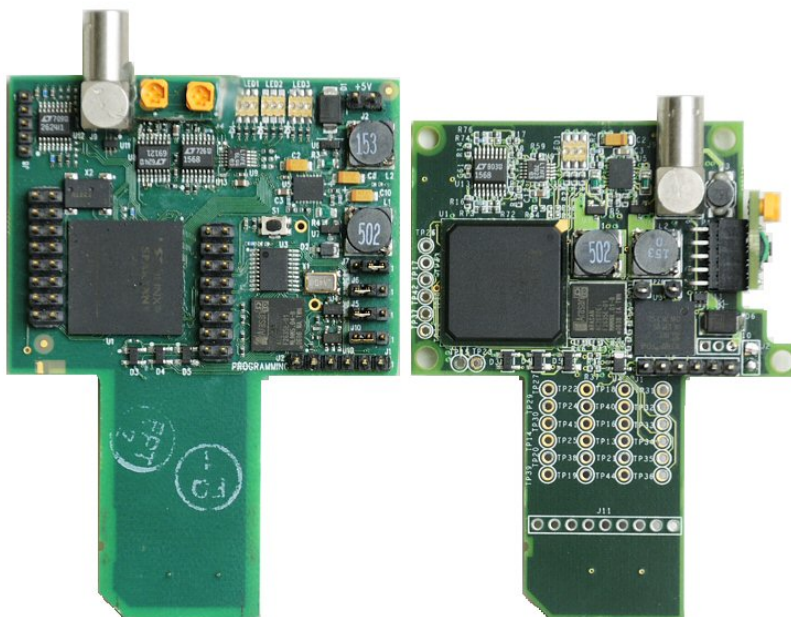
Figure 1. SDIO interface board v.2 on left and v.3 on right.

In addition to the reduction in size, the v.3 board has also had an upgrade in its FPGA that controls the onboard hardware such as ADC and SDIO interface communications, as well as its associated PROM. As shown in Table 1, the new Xilinx XC3S1500 used in v.3 of the SDIO interface board has a greater number of system gates and logic cells compared to the XC3S1000L used in v.2. The availability of larger system resources may be used in the future to implement additional real-time signal processing on board the FPGA in addition to that available by the CPU of the PDA. Furthermore, a larger PROM needed to store the FPGA configuration code was also selected, increasing the storage capacity from 4 Mbits to 8 Mbits. The new FPGA and PROM as seen on the SDIO interface board are shown in Fig. 2 along with other key components.

	XC3S1000L (v.2)	**XC3S1500 (v.3)**
System Gates	1000K	1500K
Logic Cells	17,280	29,952
Block RAM Bits	432K	576K
Distributed RAM Bits	120K	208K
Digital Clock Managers	4	4
Multipliers	24	32
I/O Standards	26	26
Max Single Ended I/O	333	487
Package	4FTG256C	4FGG320C

Table 1. Comparison table of Xilinx FPGA used in the v.2 (middle column) and v.3 (right column) boards.

The FPGA in the v.3 board boots rapidly from the configuration PROM in 8-bit wide Master (FPGA generates the configuration clock) Parallel mode whereas for the v.2 board the FPGA

booted from the PROM in Master Serial mode. An Intersil ISL8014 regulator was also added to supply the 1.8 V core voltage to the configuration PROM. A reverse polarity protection diode was added to protect against connecting the power cable in reverse.
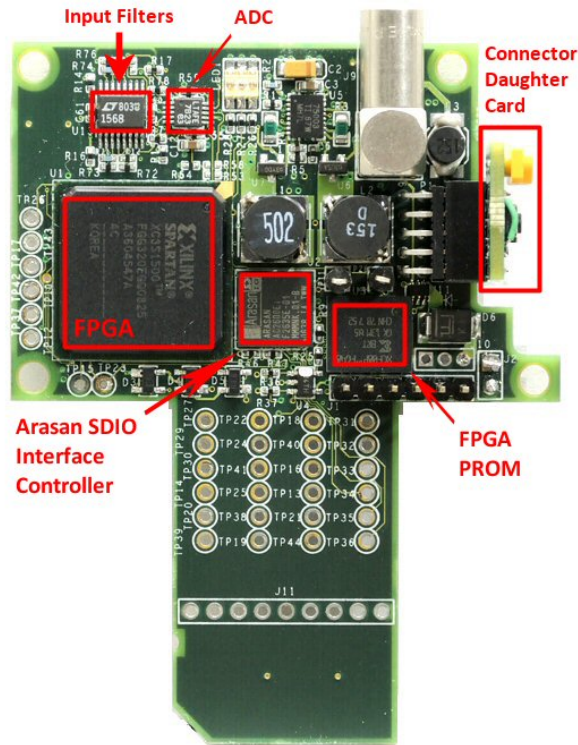

Figure 2. SDIO interface board v.3 layout.

Changes were also made to the SDIO interface board's form factor in order to change the orientation of the two cochlear connectors that attach to each of two BTEs. Rather than placing the connectors at the top most edge of the board as was the case in v.2, the two connectors have been mounted onto a daughter board that attaches to the main board at a right angle on the right most edge of the board as shown in Fig. 3. In addition to the two connectors, the reset switch has also been moved from the main board to the daughter board, also shown in Fig. 3.
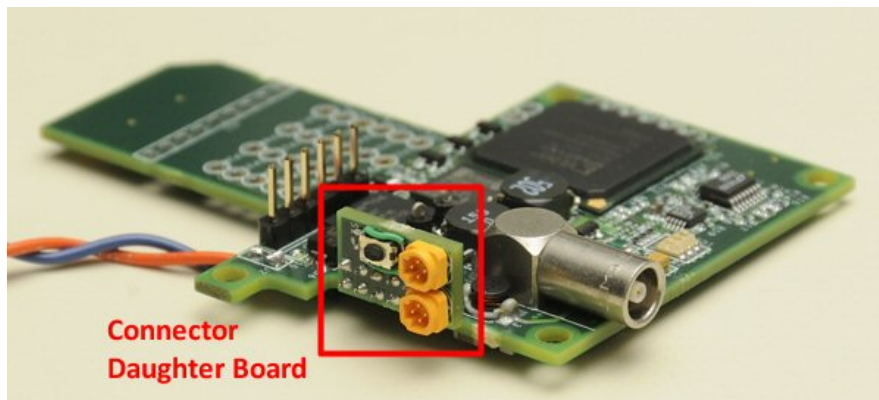

Figure 3. Details of cochlear connector daughter board.

This change in orientation to the BTE connectors was made in order to create a more user-friendly interface to the board when covered by the enclosure depicted in Fig. 4. The 3D rendering of the SDIO interface board enclosure prototype reveals a lid positioned directly above the daughter board. Users will be able to access the BTE connectors and reset switch through this lid, and once connected, the BTE cables will feed through a hole at the top, right-most corner of the enclosure that provides additional strain relief. A 3D breakout of each of the prototype enclosure panels is shown below in Fig. 5, illustrating how the various panels interconnect with one another.
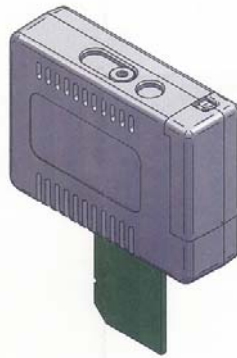

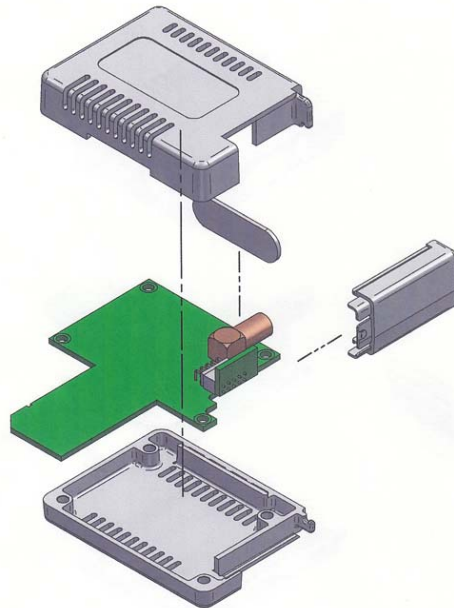**Figure 4.** 3D rendering of prototype enclosure.

Figure 5. 3D component breakout of the prototype enclosure.

The SDIO board binaural stimulation was also tested in a Verizon XV6800 PDA phone (Qualcomm MSM7500 processor at 400 MHz) with Windows Mobile 6.0 Professional operating system. The PDA phone has a microSD interface and a SD-to-microSD adapter was used as shown in Figures 6 and 7.

Figure 6. SDIO board plugged into the SD end of a SD-to-microSD adapter.

Figure 7. SD-to-microSD adapter plugged into the Verizon XV6800 phone.

In addition the High Rate stimulation mode was implemented (see QPR 10), tested and integrated with the Standard Mode. The modes can be switched by means of a parameter in the parameter file read by the PDA on program startup. Additional parameters in the startup file include pulse width, pulse rate, MCL and THR values for all electrodes, and mode of stimulation - MP1, MP2 or MP1+2. Additionally either ear can be stimulated (monaurally) or both simultaneously (binaurally).

2.2 Integrating LabVIEW code with SDIO board

In the previous QPRs (e.g., QPR1, QPR2, QPR9), we reported on the development of speech coding algorithms implemented in LabVIEW. This was done in parallel to the development of speech coding algorithms implemented in C. The LabVIEW code developed previously, however, was not integrated with the SDIO board, as it took input from the PDA microphone rather the microphone(s) on the Freedom BTE unit(s). In this quarter, we report on the integration of the LabVIEW code with the SDIO board.

C DLLs were called from within the LabVIEW environment to: (1) capture the microphone signals from the Freedom BTE units, and (2) send the envelope amplitudes to the Freedom coil via the SDIO board. Speech signals acquired by the microphones in the Freedom BTE units were passed to the PDA through the SDIO board and were processed using either a filterbank approach, an FFT approach (as done commercially) or a recursive-DFT approach all implemented in LabVIEW. The obtained channel envelopes were compressed using a logarithmic compression and mapped into the cochlear implant users' dynamic range. The compressed channel outputs were then written back onto the SDIO board and then sent to the Freedom coil.

Two implementations of ACE in LabVIEW were completed; one based on the non-recursive FFT and one based using a recursive FFT (see QPR9) approach. A paper was submitted (now accepted for publication at ICASSP'09) discussing the different versions of our implementations including different windows and different fixed-point precisions. The recursive-DFT approach required approximately 6 to 7 ms to process two frames of 256 samples (corresponding to 11.6 ms for sampling frequency of 22050 Hz) for speech captured in binaural mode. The same process with the filterbank approach required 10 to 11 ms in binaural mode.

Figure 8 shows the input (Figure 8a) and output (Figure 8b) front panels of the PDA designed using LabVIEW.
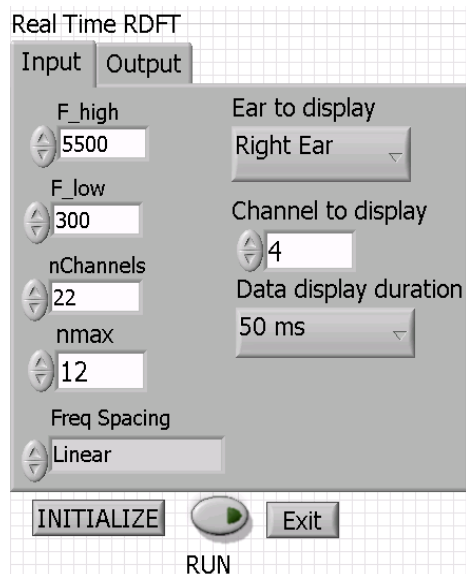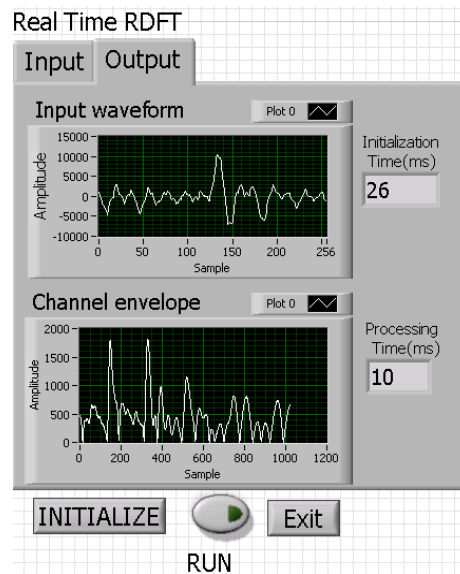
|(a) Input panel of PDA. | (b) Output panel of PDA.|

Figure 8: The PDA front panel showing the input and output tabs.

The input tab allows the user to change the following parameters affecting the CIS or ACE implementations:
1. F_high: upper cut-off frequency of last (22nd in this example) filter, corresponding to the input signal bandwidth.
2. F_low: lower cut off frequency of first filter.
3. nChannels: number of active electrodes; by default it is set to 22.
4. nmax: number of channels selected in ACE implementation; by default it is set to 12.
5. Freq Spacing: there are two options on how the nChannels are allocated in frequency.
   i.   Linear: Frequency is divided linearly into nChannels.
   ii.   Logarithm: Frequency is divided logarithmically into nChannels.

After selecting the above parameters, the user has to press the 'Initialize' button.

In the output tab (see Figure 8b), the user may observe the captured microphone signal (from left or right implant) in real-time as well as the corresponding envelope output in that channel. The user has the choice to select either 50ms or 100ms analysis channel data to display. The processing time taken to process one frame and the time taken to initialize the parameter are displayed as 'Processing time(ms)' and 'Initialization time(ms)' respectively. The parameter initialization occurs when the user presses the 'Initialize button' and then the processing of the speech starts when the user presses the 'RUN' button.

2.4 Plans for next quarter

- Continue debugging and testing the software running on the final SDIO interface board (v.3).
- Continue with the design of a new SDIO interface board for our 8-channel stimulator chip to be used for chronic animal studies.

Appendix

V. Gopalakrishna, N. Kehtarnavaz, and P. Loizou. *User's Guide: Real-Time Cochlear Implant Simulator on PDA Platforms Using Recursive DFT.*