Tenth Quarterly Progress Report

NIH-NO1-DC-6-0002

Open Architecture Research Interface for Cochlear Implants

Song Guo, Hoi Lee, Douglas Kim, Rohith Ramachandran, Nageswara R Gunupudi, Kostas Kokkinakis, Vani Gopalakrishna, Nasser Kehtarnavaz, Arthur Lobo and Philipos C. Loizou

Department of Electrical Engineering
University of Texas-Dallas
Richardson, TX 75080
Email: loizou@utdallas.edu

July 1, 2008 – September 30, 2008

1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies, a recording unit for collecting evoked potentials from human subjects and a portable processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA).

2. Summary of activities for the quarter

Work in this quarter focused on testing our 8-channel stimulator chip to be used for animal studies. We successfully tested the stimulator chip and demonstrated that it is capable of stimulating simultaneously or sequentially (interleaved) eight channels. The stimulator can be easily configured to produce symmetric biphasic pulses as well as asymmetric charge-balanced biphasic pulses. We also evaluated, using normal-hearing listeners, the PDA implementation of the beamforming algorithm developed in the last quarter (QPR9). The listening tests showed that the PDA implementation can yield significant gains in intelligibility in situations in which the target speaker and interferer signals are spatially separated. Finally, we successfully completed implementing a high-rate (up to a maximum rate of 31,500 pulses/sec) stimulation mode available in the Freedom implant (CI24RE).

2.1 Evaluation and testing of 8-channel stimulator for animal studies

A highly-configurable 8-channel current stimulator has been tested in this period. Fig. 1 shows the block diagram of our designed stimulator, which consists of a 3-bit channel selector ($A_0 - A_{2)}$, a 9-bit current amplitude selector ($B_0 - B_{8)}$ for controlling the amplitude of the stimulating pulse within each channel, two control signals (Ctrl1 and Ctr2) for controlling both the pulse width and frequency (stimulation rate) of the stimulating pulses within each channel, and a total of 8 configurable current sources to generate charge-balanced biphasic current pulses. The non-overlapping control block shown in Fig. 1 consists of logic circuitry that ensures that there is no overlapping between the $Ctrl1_{out}$ and $Ctrl2_{out}$ signals under different inputs of Ctrl1 and Ctrl2. The non-overlapping between $Ctrl1_{out}$ and $Ctrl2_{out}$ guarantees the proper function of the current source for the generation of positive and negative current pulses.

The 8-channel stimulator IC chip was fabricated with a standard 0.35μm CMOS n-well process. Figure 2 shows the setup used to test the stimulator chip. In the set up shown, the stimulator was configured for simultaneous stimulation of two channels using symmetrical charge-balanced biphasic current pulses. Figs. 3 and 4 demonstrate the detailed measurement results of the 8-channel current stimulator in different configurations. The examples in Fig. 3 demonstrate that the stimulator can generate either symmetrical (Fig. 3a) or asymmetrical (Fig. 3b) charge-balanced biphasic current pulses via the use of the Ctrl1 and Ctrl2 signals (shown it top traces of Fig. 3). The examples in Fig. 4 demonstrate that the stimulator can

deliver simultaneous (Fig. 4a) and non-simultaneous (Fig. 4b) stimulation of pulses in different channels.

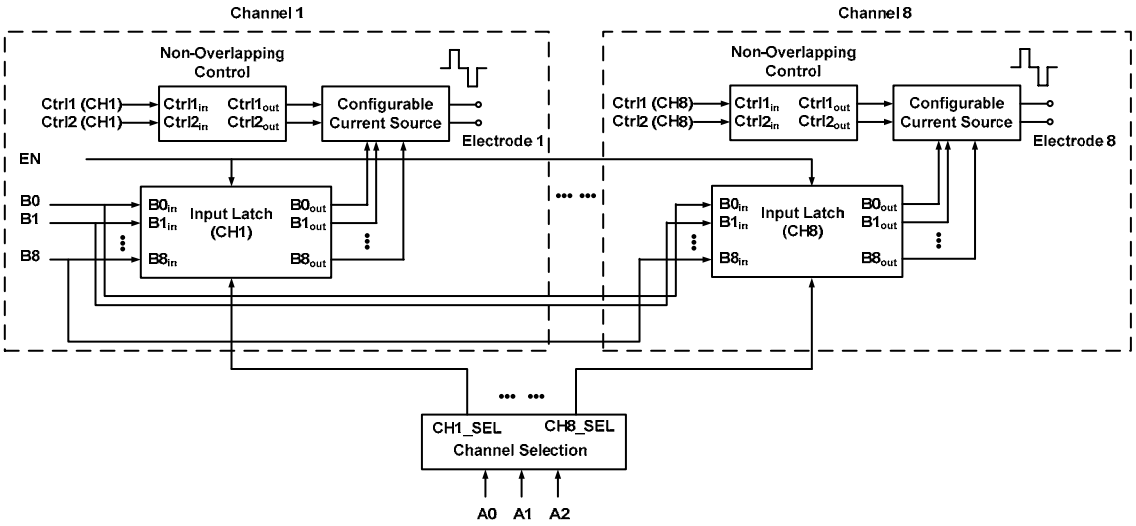


Fig. 1. Block diagram of the designed 8-channel stimulator chip.

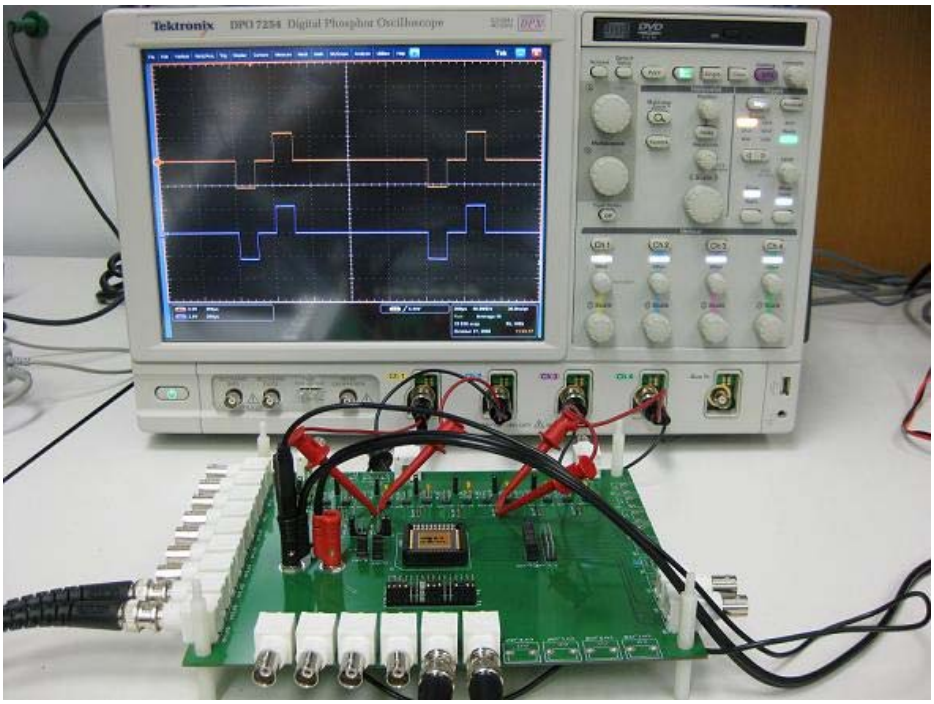
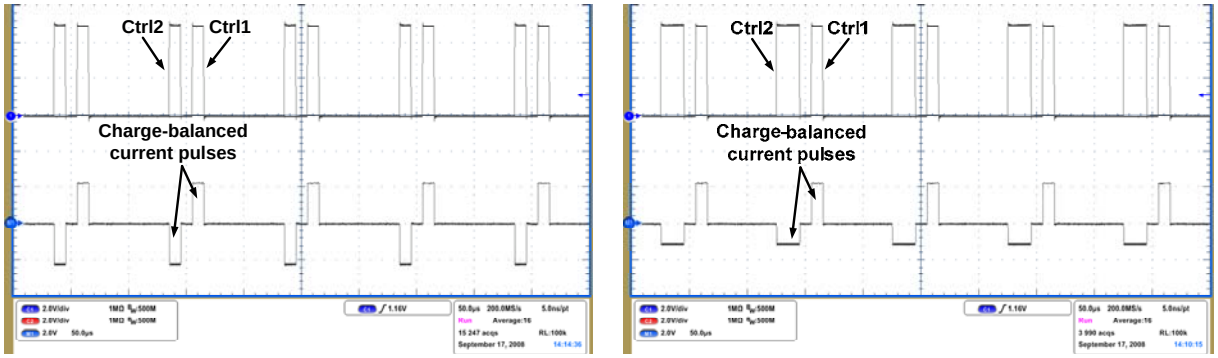
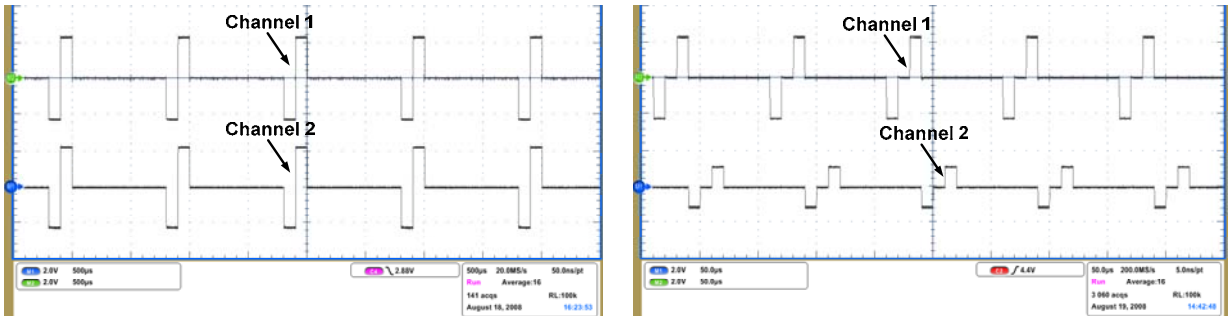


Fig. 2. Test setup of the 8-channel stimulator. The scope screen shows the simultaneous stimulation of two channels.



(a) (b)

Fig. 3. Panel (a) shows symmetric charge-balanced pulses and panel (b) shows asymmetric charge-balanced pulses generated with our stimulator chip.



(a) (b)

Fig. 4. Panel (a) shows simultaneous stimulation of two channels and panel (b) shows non-simultaneous (interleaved) stimulation of two channels.

The stimulator chip test board depicted in Figure 2, is shown in more detail in Figure 5. This board is used in the evaluation of the eight-channel bipolar current source. Adjustment of the current output level, ranging from 0 mA to 1 mA, is handled on a per channel basis, with input signals Addr0-Addr2 being used to address each of the eight current output channels. Once a channel is addressed and selected, input signals b1-b9 define a nine bit binary number associated to a current amplitude level. Output waveform generation is controlled by input signal pairs CHx_ctrl, where the subscript x refers to one of eight channels. Positive current flow is produced when the positive signal of CHx_ctrl is held high while the negative signal of CHx_ctrl is held low. Conversely, negative current flow is produced when the negative signal of CHx_ctrl is held high while the positive signal of CHx_ctrl is held low. No output current flows when both signals are held low. Varying combinations of both the current output level and the direction in which the output current flows can be used to generate a wide range of stimulus signals of varying polarity, amplitude, and pulse widths.

The control signals shown in Figures 3 and 5 are provided (for testing purposes) by digital signal generators. In the next quarter, we will work on the design of a new SDIO interface board that will house the stimulator chip and the FGPA. In this board, the control signals will be provided by the FPGA and the various stimulation modes/configurations (simultaneous vs. interleaved, stimulation rate, pulse width) will be easily programmed via the PDA.

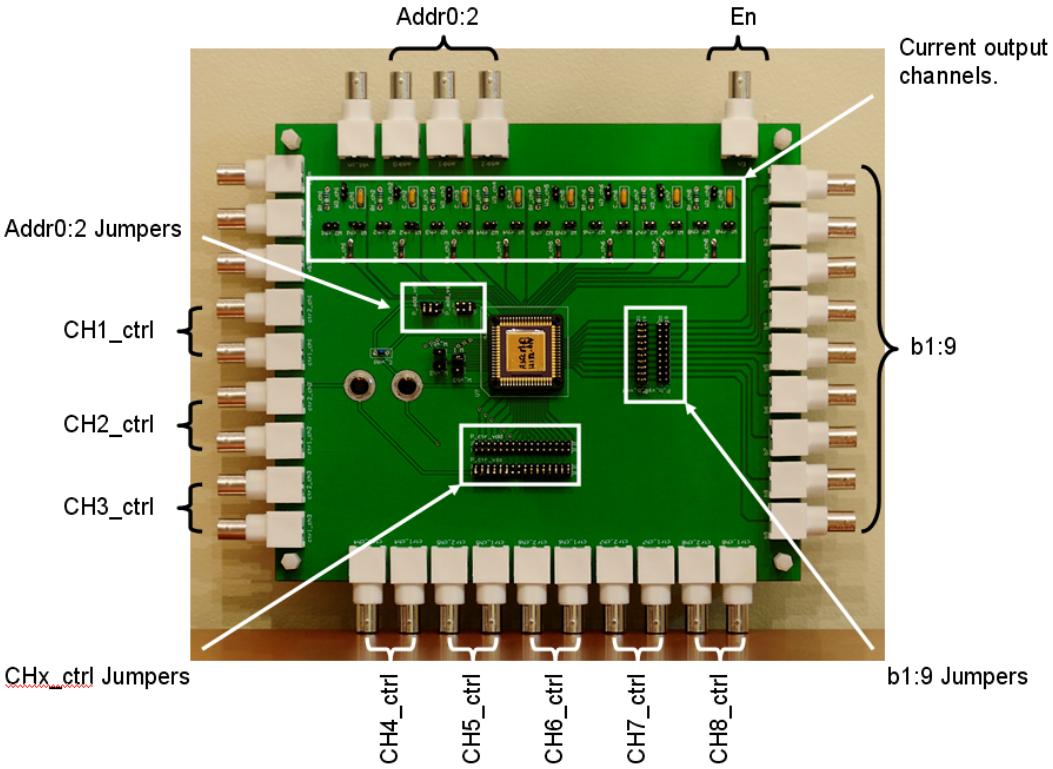


Fig. 5. Test board used for assessing functionality of the 8-channel stimulator chip.

2.2 Evaluation of beamforming algorithm for bilateral applications

In the last progress report (QPR9), we described the beamforming algorithm (Griffiths and Jim, 1982) implemented on the PDA. This algorithm was implemented to allow researchers interested in bilateral cochlear implant studies to explore variations or improvements to bilateral coding algorithms. In the present quarter, we evaluated the PDA implementation of the beamforming algorithm using normal-hearing listeners. An off-line version of the beamformer was used, which took as input recorded mixture speech files, and produced as output the beam-processed speech files.

IEEE sentences were used as test materials, and steady speech-shaped noise was used as the interferer (masker). A set of free-field-to-eardrum (or anechoic) head-related transfer functions (HRTFs) previously measured in an acoustic manikin (Head Acoustics, HMS II.3) as described in the AUDIS catalogue (Blauert *et al.*, 1998), were used to simulate different spatial locations of the speech target and interferer signals. To generate the multi-sensor composite signals observed at a pair of microphones (mounted to the left and right ears), the target and interferer stimulus for each position were convolved with the set of HRTFs for the left and right ear, respectively, thus generating a set of mixture signals for each of the two ears. The simulated target location was always at the front (0° azimuth), and the masker location was on the right (90^{o} azimuth). The interfering noise was mixed at a target-to-masker-ratio (TMR) of -5 dB. A total of twenty IEEE sentences (two lists) were processed via the beamforming algorithm implemented on the PDA.

The beam-processed files were presented diotically to the normal-hearing listeners via headphones. For comparative purposes, a different set of 20 mixture sentences (-5 dB TMR) were also presented to the listeners. The results, scored in terms of percentage of words identified correctly, are shown in Fig. 6. Mean performance obtained with unprocessed sentences was 80%. Performance obtained with the PDA implementation of the beamforming algorithm was 95%. Paired samples t-tests showed that this difference was highly significant ($p=0.006$). In brief, although this evaluation was limited in the number of spatial configurations and type of maskers used, it demonstrated that the PDA implementation of the beamforming algorithm can yield significant gains in intelligibility. Concomitant improvements in performance are expected with bilateral implant users.

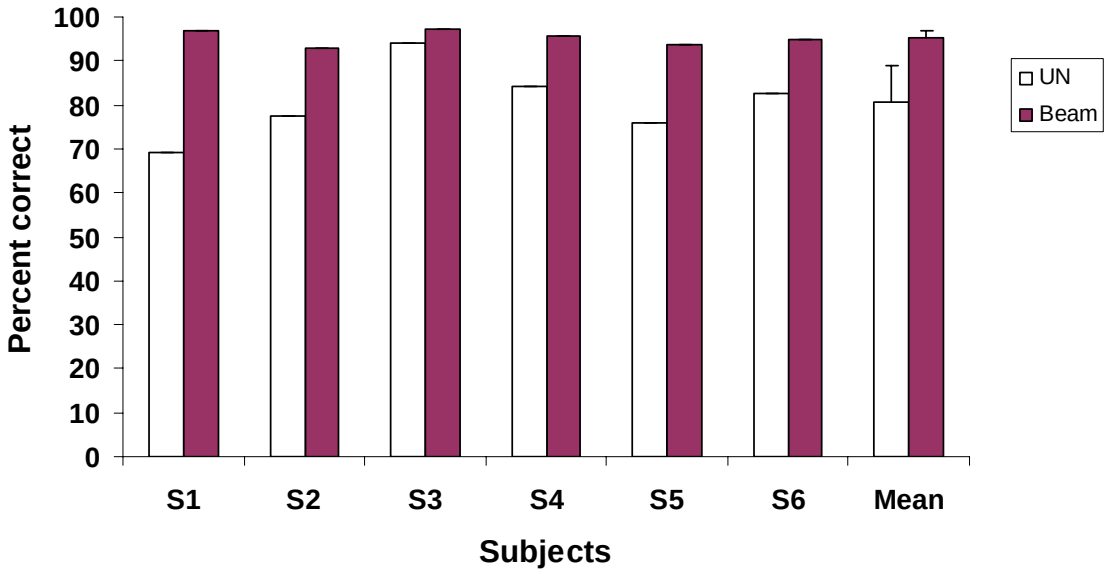


Fig. 6. Intelligibility, measured in terms of percentage of words identified correctly, of sentences (mixed at -5 dB TMR) processed via the PDA implementation of the beamforming algorithm (labeled as Beam). For comparative purposes, the intelligibility of unprocessed (labeled as UN) mixture sentences is also shown.

2.3 High-rate implementation with the Freedom (CI24RE) implant

The Freedom cochlear implant (CI24RE) supports a high-rate stimulation mode. In particular, the ACE(RE) strategy (specific only to the Freedom implant) can be implemented at an aggregate stimulation rate of 31,500 pulses/sec (note that in the standard mode, the ACE strategy operates at an aggregate rate of 14,400 pulses/sec). More precisely, the ACE(RE) strategy with 9 maximum selected, can operate at a maximum stimulation rate of 3,500 pulses/sec per channel. The pulse width is set to 9.6 μsecs.

A different protocol had to be implemented to activate the high-rate stimulation mode. The high-rate protocol has been implemented and tested successfully during the present quarter.

2.4 Other Activities

- Dr. Bas van Dijk, the global research coordinator for Cochlear's Technology Center in Europe (Belgium), visited our lab. An overview of our lab activities, including a PDA binaural stimulation demo, was given to Dr. Dijk during his visit.
- We received the final SDIO interface board, and are currently debugging it.
- Prepared and submitted a conference paper (see Appendix) for work done in the previous quarter (QPR9) on optimization of the recursive FFT implementation.

2.5 Plans for next quarter

- Continue debugging and testing the final SDIO interface board.
- Design a new SDIO interface board for our 8-channel stimulator chip to be used for chronic animal studies.
- Integrate our LabVIEW software implementation with existing software running on the SDIO interface board.

Acknowledgments

We would like to thank Mr. Clemens Zweekhorst, from Cochlear's Technology Center in Belgium, for all his help and technical support he provided regarding the Freedom cochlear implant (CI24RE).

References

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Griffiths, L and Jim, C. (1982). "An alternative approach to linearly constrained adaptive beamforming," *IEEE Trans Antennas Propagation*," AP-30, 27-34.

Appendix

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