A 9-Bit Configurable Current Source with Enhanced Output Resistance for Cochlear Stimulators

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Abstract - **This paper presents a configurable current source for cochlear stimulators. A switchable multi-bias active-cascode architecture is developed to provide a 9-bit output current in a small implementation area. A stacking MOS structure enables the current source to achieve high output resistance and large voltage compliance. Implemented in a standard 0.35μm CMOS process, the current source can source a maximum 1mA current, provide ≥4.77V voltage compliance under a 5V supply and achieve >50MΩ output resistance in 0.26mm^2.**

I. Introduction

Cochlear implants are well-accepted prosthetic devices to restore hearing to profoundly deaf people by delivering electrical stimuli to auditory nerves. Fig. 1 shows a structure of a cochlear implant [1], which consists of an external module and an implanted system. In the implant, a current stimulator consisting of current source(s) is used to generate biphasic charge-balanced current pulses with a suitable amplitude, period and pulse width configured by the decoder to stimulate auditory nerves through an electrode array such that hearing can be restored. Since hearing restoration is determined by the quality of the current pulses, the performances of the current source in the stimulator are crucial. Studies have found that large amplitude of 1mA anodic or cathodic stimulus current generated by the current source is needed to elicit auditory percept under variations in stimulation types (bipolar or monopolar), placement of electrodes, number of remaining ganglion cells, etc [2]. In addition, the output current of the current source should have large amplitude resolution such that the cochlear implant could be more flexible to be adjusted under variability in patient thresholds for comfortable stimulation levels. However, with the increase in the amplitude resolution, the implementation area of the current source greatly increases. Large implementation area can lead to errors in gradients, edge effects, etc during the chip fabrication, which degrades the accuracy of the output current. Moreover, the current source should have high output resistance with large voltage compliance to ensure accuracy of the output current under variations of the electrode impedance. Unfortunately, the above performance requirements of the current source are very challenging to achieve simultaneously.

Previous reported current sources either for retinal [3] or cochlear [4], [5] stimulators are based on a wide-swing cascode topology [3], [4] or voltage-controlled resistors (VCR) [5]. To achieve small chip area, the output resistance of the reported wide-swing cascoded current source is only about hundreds of kΩ due to the use of small-size transistors and the resulting channel-length modulation effect [3]. On the other hand, the output resistance of the reported VCR current source can achieve over 10MΩ [5]. In the VCR current source, different current amplitudes is generated by varying the gate-to-source voltage of a triode-region transistor. However, the intrinsic non-linear behavior between current and gate-to-source voltage of the triode-region transistor limits the current amplitude resolution in the VCR current source.

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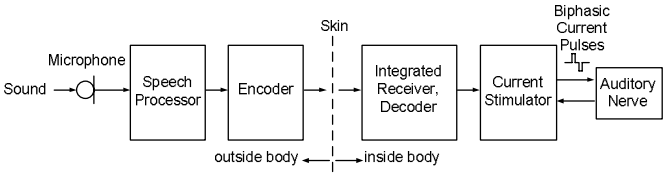

Fig. 1. Structure of a cochlear implant system.

This paper presents a current source using a switchable multi-bias active-cascode digital-to-analog converter (DAC), which can source/sink a 1mA full-scale output current with 9-bit configurable amplitudes in a small implementation area. A stacking MOS structure is also developed to allow the current source to achieve large output resistance with a wide voltage compliance range. Table I provides performance comparisons of different current sources for current stimulators. Compared to all reported current sources, the proposed current source achieves the largest output current, amplitude resolution, voltage compliance and output resistance, while small implementation area can still be maintained. Details of the proposed current source will be discussed in later sections of this paper.

II. Proposed Current Source

The proposed current source is the core of a 8-channel bipolar current stimulator in our portable cochlear implant research platform for animal studies [6]. Fig. 2 shows a conceptual diagram of a single-channel bipolar current stimulator, in which two control signals are used to determine on/off of switches SW_{s1} – SW_{s4} for generating biphasic current pulses between two adjacent electrode sites A and B. In particular, during anodic (cathodic)-pulse phase, SW_{s1} (SW_{s2}) and SW_{s4} (SW_{s3}) allow the current sinking from site A (B) to site B (A) through the auditory nerve. Since the biphasic

TABLE I
PERFORMANCE COMPARISONS WITH PREVIOUSLY REPORTED CURRENT SOURCES

	JSSC 03 [3]	JSSC 06 [4]	TBME 05 [5]	**This Work**
Supply Voltage	±5	±2.5	5	**+5**
Maximum Output Current (mA)	0.4	0.5	0.21	**1**
Resolution	8 bits	8 bits	5 bits	**9 bits**
Maximum INL (LSB)	-3.11	N.A.	N.A.	**2.9**
Maximum DNL (LSB)	2.15	N.A.	N.A.	**0.8**
Voltage Compliance (V)	3.6V (cathodic current) 3.35V (anodic current)	±2.0	4.25	**4.77**
Output Resistance (MΩ)	0.443	N.A.	>10	**>50**
Area (mm^2)	0.227	N.A.	0.05	**0.26**
Technology	standard 1.2µm CMOS	High-voltage 0.5µm CMOS with thick gate oxide	standard 1.5µm CMOS	**standard 0.35µm CMOS**

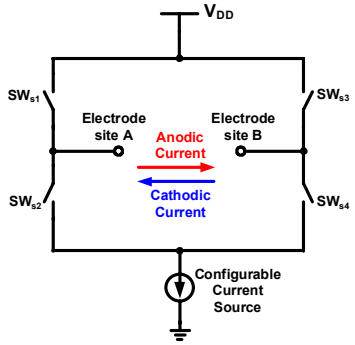

Fig. 2. Conceptual diagram of a bipolar current stimulator.

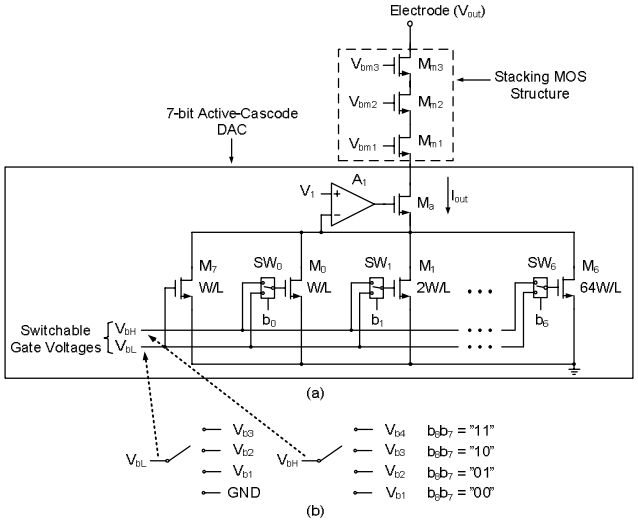

Fig. 3. (a) Structure of the proposed configurable current source with its (b) 2-bit switchable bias scheme.

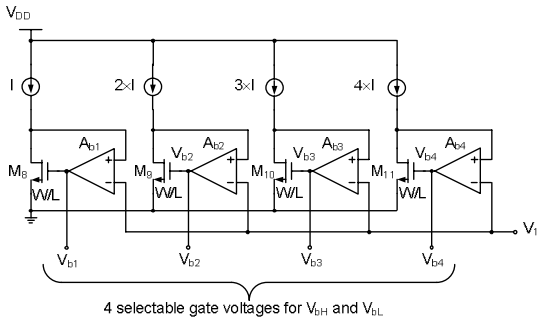

Fig. 4. Bias voltage generation circuit.

current pulses are provided by the same current source, charge balance can be achieved and the current source determines the performances of the current stimulator.

A. Structure and Operational Principle

Fig. 3(a) shows the structure of the proposed current source, which consists of an active-cascode 7-bit current-mode DAC realized by transistors M_a, M_0 - M_6 and an amplifier A_1. The active-cascode architecture can provide high resistance at the drain of M_a. Input control code of the DAC $b_0 – b_6$ is used to connect gate voltages of M_0 - M_6 to either V_{bH} or V_{bL} through switches $SW_0 – SW_6$. For example, the gate voltage of M_n is connected to V_{bL} (V_{bH}) through SW_n when $b_n = 0$ (1), where n is from 0 to 6. Fig. 3(b) shows a 2-bit switchable bias scheme, which allows gate voltages V_{bL} and V_{bH} of $M_0 – M_7$ to select from different bias voltages $V_{b1} – V_{b4}$ based on an input control code b_8b_7. Voltages $V_{b1} – V_{b4}$ are provided by the bias voltage generation circuit shown in Fig. 4, in which current I is the least significant bit of the output current I_{out}.

To generate the first 7-bit output current I_{out}, $b_8b_7 = 00$ and thus V_{bL} and V_{bH} are connected to 0 and V_{b1}, respectively. With high-gain amplifiers A_1 and A_{b1}, the drain voltages of $M_0 – M_8$ are maintained to be the same. Since all $M_0 – M_8$ are designed to operate in the saturation region, the current from M_8 can be accurately mirrored to transistors M_n when $b_n = 1$ as

$$I_n = 2^n I \quad . \qquad (1)$$

Therefore, the active-cascode DAC is binary-weighted to realize a 7-bit output current I_{out} as

$$I_{out} = I(b_0 + 2b_1 + 2^2 b_2 + 2^3 b_3 + 2^4 b_4 + 2^5 b_5 + 2^6 b_6) \quad . \qquad (2)$$

By controlling $b_0 – b_6$ to be either 1 or 0, the output-current ranging from 0 to 127I can be generated.

In order to achieve 9-bit resolution, the 2-bit switchable multi-bias scheme selects appropriate gate voltages for $M_0 – M_7$ based on the input control code b_8b_7 = 00, 01, 10, or 11. As described above, when b_8b_7 = 00, the dynamic range of I_{out} is from 0 to 127I. When the input code increases from 127 to 128, b_8b_7 changes from 00 to 01 to cause $V_{bL} = V_{b1}$. It allows the gate voltage of $M_0 – M_6$ to remain at V_{b1} when $b_0 – b_6 = 0$. I_{out} due to $M_0 – M_6$ is thus still kept at 127I. The compensation transistor M_7 provides an additional I to allow the total I_{out} of the current source smoothly increasing from 127I to 128I. Therefore, with $b_8b_7 = 01$, the dynamic range of I_{out} from 128I to 255I can be realized by setting different

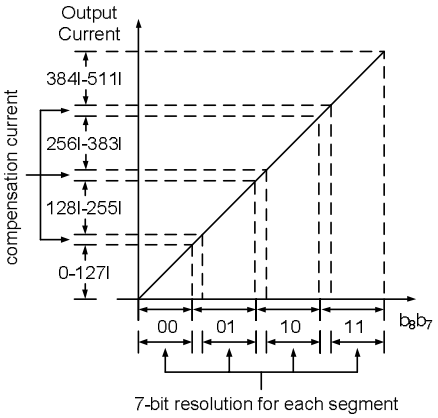

Fig. 5. Relationship between output current and 2 additional bits.

values of $b_0 - b_6$. Similarly, the output current from 256I to 383I and from 384I to 511I can also be generated by the proposed 2-bit switchable multi-bias strategy and 7-bit current-mode DAC with monotonic increasing behavior shown in Fig. 5. The compensation transistor M_7 is important to ensure smooth transitions between two different 7-bit segments of the output current.

The implementation area of the proposed current source is greatly reduced by the proposed 2-bit switchable bias generation scheme. In the 7-bit current-mode binary-weighted DAC shown in Fig. 3(a), the large-size transistor M_6 occupies almost half of the total implementation area of transistors $M_0 - M_6$. Obviously, if a conventional 9-bit binary-weighted DAC structure is adopted by using two additional large transistors with sizes of 128(W/L) and 256(W/L), the total implementation area would be about 4 times as that of the existing 7-bit DAC structure. It should be noted that the area occupied by the 2-bit switchable bias generation scheme is compact due to the use of small-size transistors. The proposed current source based on switchable multi-bias 7-bit current-mode DAC architecture is thus an area-efficient way to realize 9-bit current amplitude resolution. The compact design of the proposed current source also provides good current matching and linearity of the output current.

B. Output Resistance & Voltage Compliance Considerations

The output resistance of the active-cascode DAC is given by

$$R_o = A \cdot g_{ma} r_{o1} r_{oa} \tag{3}$$

where A is the gain of amplifier A_1, r_{o1} is the equivalent output resistance of transistors M_0 - M_7, and g_{ma} and r_{oa} are the transconductance and output resistance of M_a, respectively. Since V_1 is large enough (~0.18V) to ensure all transistors $M_0 - M_7$ in the saturation region, the output resistance R_o is A times larger than that of wide-swing or fully cascode current sources, where A >> 1. Although the output resistance R_o of VCR current source in [5] has a similar expression as (3), its R_o value is limited by the resistance of the triode-region transistor. As a result, the proposed active-cascode DAC structure can provide the largest output resistance.

However, as the input supply of the current source as high as 5V is needed in the stimulator, the drain voltage of M_a can be close to 5V. When drain-to-source voltage $V_{ds,Ma}$ of M_a is much larger than the overdrive voltage $V_{ov,Ma}$, transistor M_a will suffer from the hot carrier effects [7]. The drain-to-substrate current $I_{DB,Ma}$ of M_a will then be greatly increased, thereby decreasing the output resistance of M_a (r_{oa}) and then the value of R_o. As shown in Fig. 6, the simulated output current of the current source (without stacking MOS structure) increases when the output voltage is beyond 3V, which indicates the decrease in the output resistance of the current source under hot carrier effects. In fact, hot-carrier effects have more serious impact on a transistor implemented in a standard sub-micron CMOS process than a transistor realized either by a high-voltage or a long-channel process due to larger electric field at the drain of a standard sub-micron CMOS transistor. It implies that it is difficult for the current source to maintain at high output resistance over a wide range of the voltage compliance under a high supply voltage and using a standard sub-micron CMOS process.

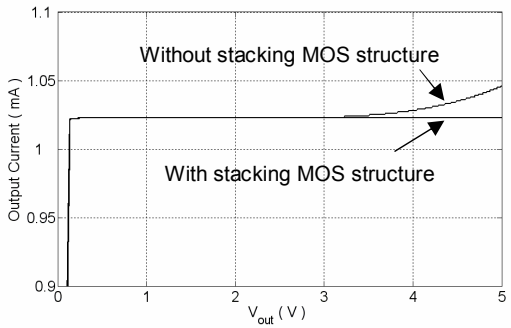

Fig. 6. Simulated output current under different output voltages.

In the proposed current source, a stacking MOS structure shown in Fig. 3(a) using transistor $M_{m1} - M_{m3}$ on top of the active-cascode DAC is developed to address the above technical challenge. The purpose of three transistors $M_{m1} - M_{m3}$ is to limit drain-to-source voltage V_{ds} across each transistor to a reasonably small value for eliminating hot carrier effects and minimizing substrate current of each transistor when the output voltage V_{out} of the current source is close to the supply rail. It should be noted that when V_{out} is small, M_{m1} - M_{m3} will be driven to the deep linear region with a very small voltage drop across the stacking MOS structure. The output resistance of the current source is guaranteed to achieve at least R_o given in (3), as transistors M_a and $M_0 - M_{11}$ are all in the saturation region. When V_{out} is large, transistors $M_{m1} - M_{m3}$ would operate in the saturation region to further increase the output resistance of the current source. From Fig. 6, the simulated output current of the proposed current source is maintained constant under a wide range of V_{out}. High output resistance with an extended voltage compliance is thus achieved in the proposed current source under a high supply voltage of 5V and a standard 0.35μm CMOS process by using the proposed stacking MOS structure.

C. Circuit Implementations

In the proposed current source, amplifiers A_1, $A_{b1} - A_{b4}$ are crucial to its output resistance and the accuracy of mirroring current. A single-stage folded-cascode structure with

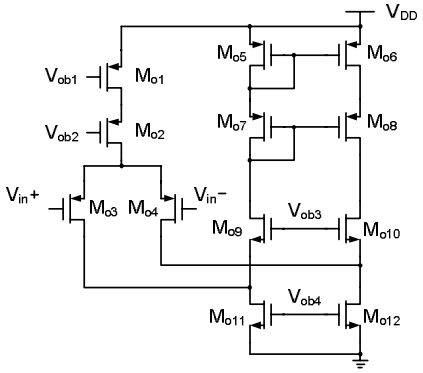

Fig. 7. Operational amplifier in the proposed current source.

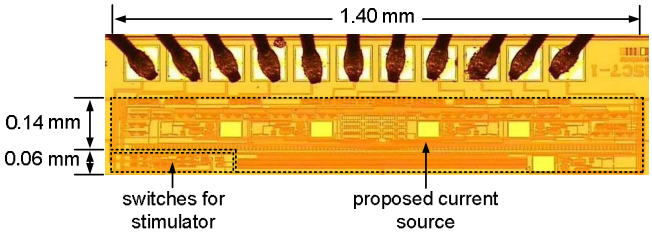

Fig. 8. Micrograph of a single-channel current stimulator with the proposed current source.

transistors M_{o1} – M_{o12} shown in Fig. 7 is used to implement A_1, A_{b1} – A_{b4} for achieving high low-frequency gain. Since V_1 at the positive terminal of A_1 is a low voltage for minimizing the drain-to-source voltage of transistors M_0 – M_{11} and maximizing the voltage compliance of the current source, the input differential pair of A_1 is realized by pMOS transistors M_{o3} and M_{o4}. With a 5V input supply, a cascode current mirror with transistors M_{o5} – M_{o8} can provide high output resistance at the amplifier output across its output swing.

III. Measurement Results

In order to verify the performances of the proposed current source, a single-channel bipolar current stimulator is realized in a standard 5-V 0.35µm process. With the same concept shown in Fig. 2, the single-channel stimulator can generate biphasic current pulses to the auditory nerve by using the proposed current source. Fig. 7 shows the micrograph of the current stimulator, in which the chip area of the proposed current source is 0.26mm^2.

Table I provides the detailed measurement results. The proposed current source can source a maximum 1mA output current with 9-bit resolution. In particular, Fig. 9 shows the measured output currents of the proposed current source under different output voltages and input digital codes. The measured output resistance is at least 50MΩ for the output voltage between 0.23V and 5V. It justifies that both high output resistance and wide voltage compliance are achieved simultaneously in the proposed current source.

Fig. 10 shows the measured current pulses generated by the current stimulator. With two control signals to define on/off of switches in the stimulator, charge-balanced biphasic current pulses with the pulse amplitude of 1022µA are generated.

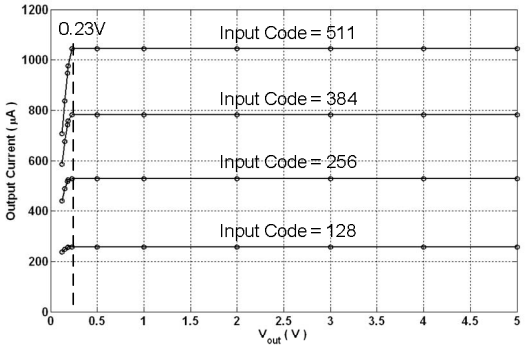

Fig. 9. Measured output current under different output voltages.

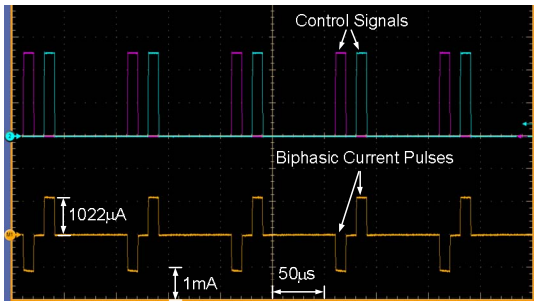

Fig. 10. Measured charge-balanced biphasic current pulses using a single-channel bipolar current stimulator.

IV. Conclusion

A 9-bit configurable current source using the proposed active-cascode 7-bit binary-weighted DAC and 2-bit switchable multi-bias scheme has been introduced and verified on silicon. The active-cascode DAC increases the output resistance, whereas 2-bit switchable multi-bias strategy helps to decrease the implementation area of the current source. Additionally, a stacking MOS structure on top of the DAC allows the current source to maintain high resistance over a wide voltage compliance range. The proposed current source is suitable for the current stimulation in cochlear implants.

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