Final Report

NIH-NO1-DC-6-0002

Open Architecture Research Interface for Cochlear Implants

Philipos C. Loizou, Arthur Lobo[†], Douglas Kim, Nageswara R Gunupudi, Vanishree Gopalakrishna, Nasser Kehtarnavaz, Hoi Lee, Song Guo and Hussnain Ali

Department of Electrical Engineering

University of Texas-Dallas

Richardson, TX 75080

Email: loizou@utdallas.edu

http://www.utdallas.edu/~loizou/cimplants/

[†] Signals and Sensors Research, Inc, McKinney, TX

April 1 2006 – March 31, 2011

Table of Contents

1. Introduction

The main aim of this project is to develop a research interface platform which can be used by researchers interested in exploring new ideas to improve cochlear implant devices. This research platform includes a stimulator unit which can be used for electrical stimulation in animal studies and a portable speech processor for implementing and evaluating novel speech processing algorithms after long-term use. The research platform chosen for this project is the personal digital assistant (PDA). This report presents the summary of our activities during the contract. All progress reports and publications generated from this contract are posted on our website (http://www.utdallas.edu/~loizou/cimplants/).

2. Speech Processor

2.1 Overview

Current CI users carry either a body-worn speech processor or a Behind-The-Ear (BTE) processor. The headpiece or BTE contains the microphone and RF transmitter, and is connected to the body-worn processor by a custom cable. Sound is picked up by the microphone and sent to the processor, which processes the signal in a way that mimics the auditory signal processing performed by the inner ear. The processor sends electrical stimulation information (e.g., pulse width, envelope amplitudes, etc.) back to the RF transmitter through the same cable. The electrode and amplitude information (reflecting current amplitude levels) is transmitted via RF through the skin to the implanted RF receiver, which in turn decodes the information and sends electrical stimulation to the electrode array implanted in the inner ear.

The main difference between what is currently available in the market and the developed speech processor is the replacement of the body-worn or BTE processor with the PDA and FGPA-interface board. Note that the FDA-approved RF transmitter, containing the transmitting coil, is the same in both cases. This interface board was custom designed in our lab.

The main function of the PDA is to process the acoustic signal picked up by the microphone, which is located in the BTE. There are a number of signal processing algorithms that can be implemented on the PDA (see review in Loizou, 1998). Typically, the CI signal processing involves filtering the signal into a number of bands (12-22), and estimating the envelope (energy) in each band. Figure 1 shows an example of such algorithm using as input the speech syllable /s a/. In this example, the signal is filtered into 4 bands, but in general the number of bands depends on the number of available electrodes implanted in the inner ear. For the Cochlear Corporation implant, used in our case, the total number of electrodes is 22. The Advanced Encoder Strategy

(ACE) is currently used in the commercial Freedom speech processor (Vandali *et al*., 2000) by most (if not all) users fitted with the 22-electrode array manufactured by Cochlear Corporation.

There are a number of reasons for choosing the PDA as the computing platform. First, it is light weight (4-6 oz), small in size and therefore portable. Second, it uses a powerful microprocessor, with the majority of the PDAs using Intel's PXA2700 processor. Some PDA models presently operate at clocks as high as 624 MHz. Third, the software running on the PDA operates under the Windows Mobile environment. As such, researchers can program novel sound processing strategies using a high-level language (C/C++). This is important as it offers flexibility and ease in terms of implementing and testing new algorithms for cochlear implants at a relatively short time, as opposed to doing the implementation in assembly language. Fourth, the PDA platform is easily "adaptable" to new and emerging technologies as they become available. That is, researchers will only need to update the software drivers rather than the hardware, as more powerful and more energy efficient chips become available in the PDA market.

Figure 1 provides a general overview of the signal flow. The acoustic signal is picked up by the microphone located in the BTE and sent to the FPGA interface board. The interface board samples the signal binaurally at a rate of 22 kHz/channel and sends the sampled (digital) signal to the PDA via the SD slot. The PDA processes the digital signal via a speech coding algorithm (e.g., ACE) and produces a set of amplitudes representing the energy levels in each band. A total of *n* amplitudes are transmitted. Note that *n*=22 in our case corresponding to the total number of electrodes available in the Cochlear Corporation's implant. The set of amplitudes are sent to the interface board via the SD slot. An FPGA (Xilinx Spartan XC3S1000L) on the interface board receives the envelope amplitudes and prepares them for transmission using an RF data communication protocol (Daly and McDermott, 1998). The FPGA sends, via the cable, a stream of RF bursts containing information about the current levels (amplitudes) to be used to stimulate each electrode along with a set of stimulation parameters, such as pulse duration and mode of stimulation (bipolar vs. monopolar). The latter set of parameters is used by the implanted RF decoder for constructing biphasic pulses.

A number of mechanisms have been set in place to ensure the safety of the patients and these are described in more detail in the next section. Foremost among those mechanisms is providing no access to the source code running on the interface board. *The code running on the FPGA will be saved in PROM and researchers will not be able to modify it in any way*. This is done to ensure that the cochlear implant patients will not be overly stimulated. Secondly, software safety checks are set in place on the PDA side for checking: (1) the range of envelope amplitudes and (2) the range of stimulation parameters (e.g., pulse width) to ensure that they fall within the permissible and safe range. *Researchers will not have access to the safety-checking software. Only stimulation parameters that have already been approved by the FDA and are currently in use by patients will be allowed.*

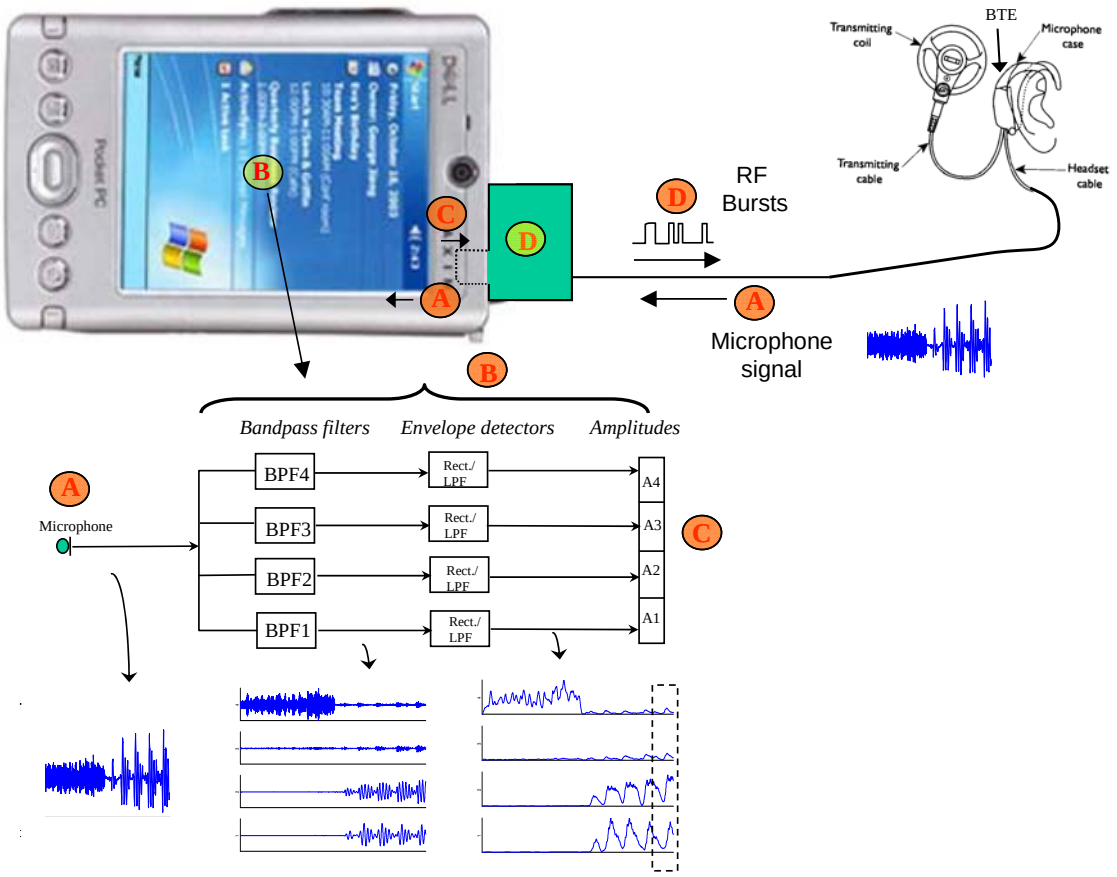

Figure 1 A schematic of the signal flow in the PDA speech processor. The acoustic signal is picked up by the microphone (A), sent (via cable) to the FPGA interface board (D), which is then sent to the PDA. The PDA (B) processes the signal and generates a set (one for each channel of stimulation) of amplitudes (C). The amplitudes are sent to the FPGA interface board (D), which are then prepared for transmission to the cochlear implant in the form of RF bursts (D).

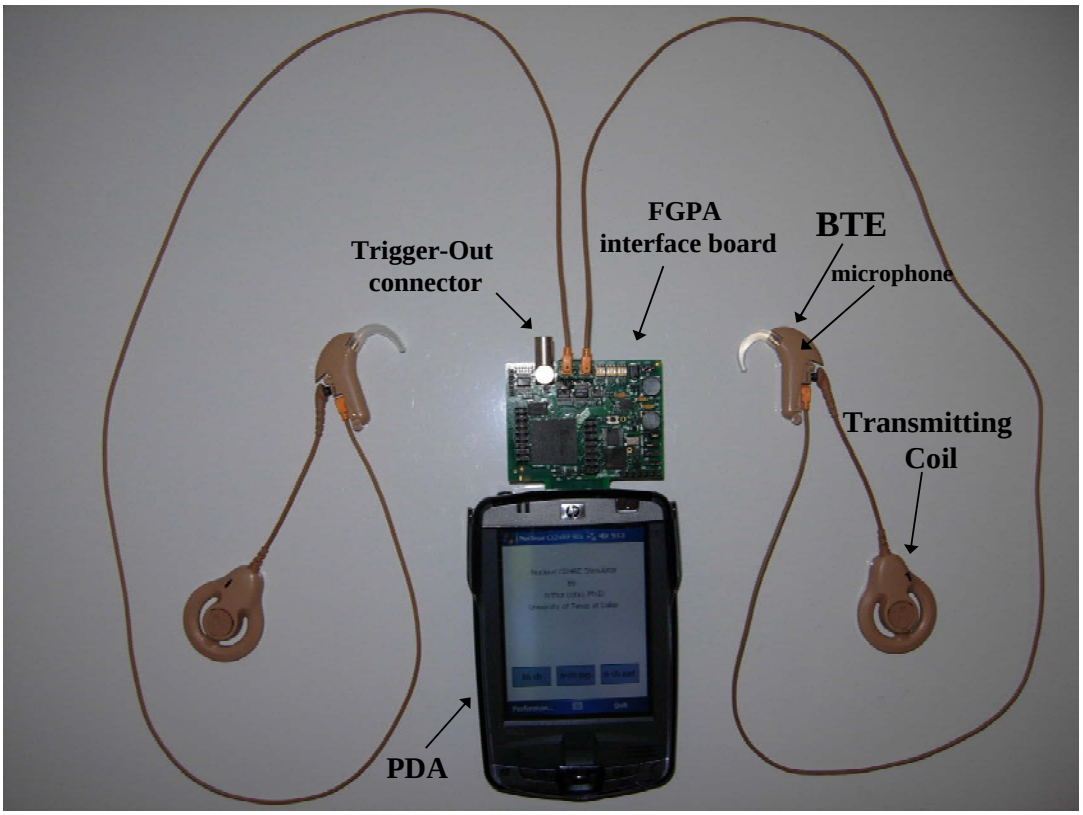

Figure 2 Picture of FPGA interface board plugged into the PDA. Two Nucleus-24 headsets (one for each ear) consisting of the BTE (containing the microphone), transmitting coil and cables are also shown.

2.2 Hardware Development

An interface board (Fig. 2) was developed for communicating and interfacing with the Cochlear Corporation's cochlear implants (including both CI22 and CI24 generations). This board plugs into the Secure Digital Input Output (SDIO) slot of the PDA and enables the PDA to stimulate the Cochlear Corporation's CI24 or CI22 implant. Very briefly, the PDA sends stimulus amplitude packets to the SDIO card using the SDIO 4-bit communication protocol. The amplitudes are converted by the FPGA to the embedded protocol (Daly and McDermott, 1998) for the CI24 implant or the expanded protocol (Crosby *et al.*, 1985) for the CI22 implant, and finally sent to stimulate the implant via the Freedom Coil.

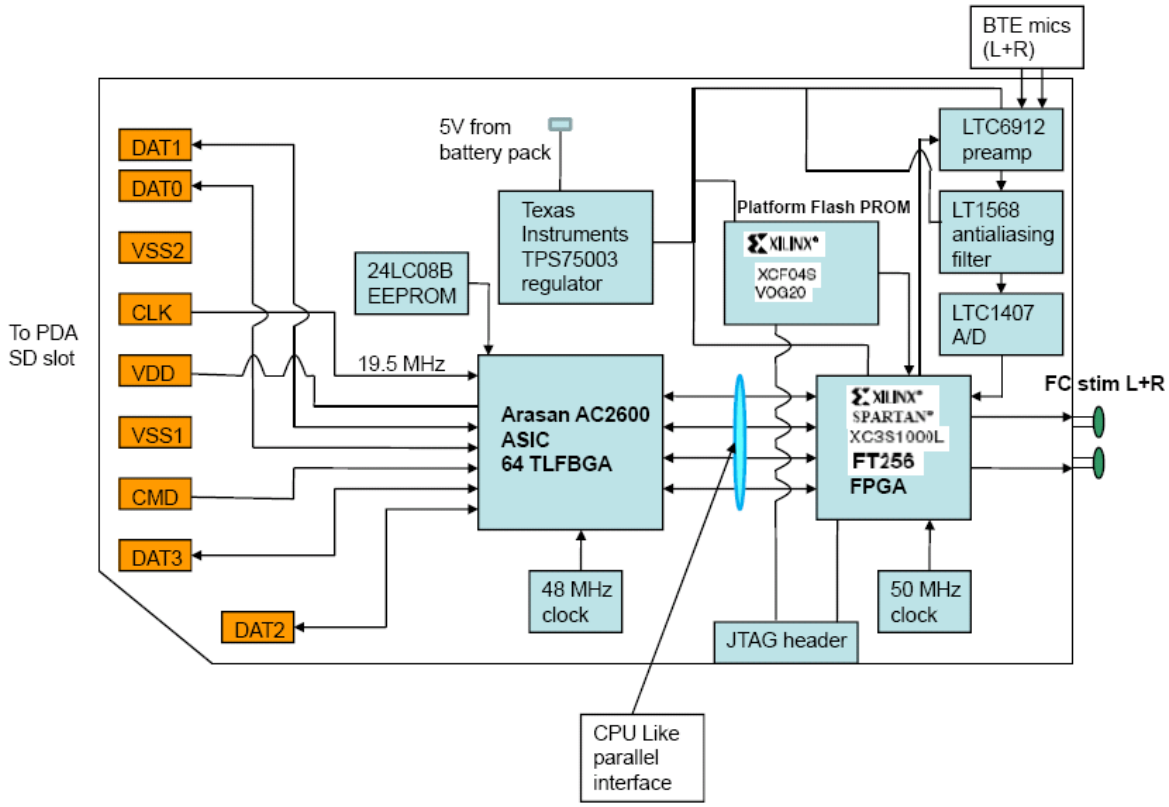

Figure 3 Functional diagram of FPGA interface board.

Figure 3 shows the functional diagram of the FGPA board consisting of the following components:

Arasan AC2600 ASIC

The Arasan ASIC is a SDIO card controller and implements the SDIO standard 1.2 and SD Physical Layer specification 1.10. It communicates with the SDIO host controller on the PXA270 processor in the PDA via a command response interface.

The FPGA has a Receive from A/D state machine (SM) running in parallel with a FPGA-PDA communication SM and operating off a 48 MHz clock (mem_clk) from the AC2600 ASIC. The Receive from A/D SM initializes the preamplifier gains before acquiring samples from the A/D. The incoming samples are buffered and transferred to the AC2600 in 16-bit parallel mode via the CPU-Like interface. The CPU-Like interface consists of the control lines mem_rd_lo, mem_rd_wr_hi and mem_wr_lo which are asserted when the IO_RW_EXTENDED (CMD53) SDIO command is issued by the PDA. The mem_rd_lo, mem_rd_wr_hi and mem_wr_lo lines are asserted for twice the number of mem_clk cycles used to transfer the number of data bytes requested, where two bytes are transferred per cycle. Half of the mem_clk cycles are used by the FPGA to acknowledge read or write transfers via the mem_rd_wr_vld line.

The FPGA buffer length is 256 16-bit samples/channel for the L and R channels and the sampled data is transmitted every 11.6 ms to the PDA.

Interrupt mechanism:

The transfer is initiated by a PDA-issued Read interrupt. The PDA receives the microphone sample payload in a thread, processes it with CIS or ACE strategies binaurally and transmits the stimulus amplitudes for the L and R channels in the same thread to the FPGA via the write interrupt. On the FPGA side, the FPGA-PDA communication SM receives the PDA interrupts, processes them and generates its own interrupt, mem_intr to the AC2600, using the Bus Functional Model (BFM) of the CPU-Like interface. The BFM is implemented on the FPGA and consists of the Interrupt Enable Register, the Interrupt Status Register (ISR), the Transmit Count Register (TCR), the Receive Count Register and the Data Port Register. The PDA addresses the BFM registers using the SDIO client driver with the addresses appearing on the AC2600 address lines. When the mem_intr interrupt from the FPGA is detected in the interrupt pending register of the Card Common Control Registers (CCCR) of the AC2600, the PDA reads the FPGA ISR to verify the interrupt and then issues the appropriate CMD53 (read or write) command. For the read transfer, the TCR is read to determine the block size for the CMD53 command. The mem_intr interrupt is de-asserted by the FPGA when the mem_rd_lo or mem_wr_lo asserted state is detected.

24LC08B I2C EEPROM

The 24LC08B EEPROM stores the initialization parameters for the ASIC to startup in CPU Like interface mode. The EEPROM communicates with the ASIC via an I2C bus.

Xilinx XC3S1000L FPGA

The Xilinx FPGA receives the amplitude packets from the ASIC and converts them to the Embedded protocol. The Embedded protocol bit stream is sent to the Freedom coil using a 5 MHz data signaling clock. The FPGA is clocked by a 50 MHz crystal. The FPGA logic implements a receive and transmit state machine and can support the 0.94 Mbps data link to the Freedom coil in the low rate stimulation mode using 5 cycles per cell. The peak stimulation rate is 15,151 pulses/sec. Using 4 cycles per cell the peak stimulation rate can be increased to 19,608 pulses/sec. The FPGA board can be used for bilateral (or unilateral) cochlear implant studies.

Xilinx XCF04S Platform Flash PROM

The Xilinx XCF04S is a Platform Flash PROM which stores the synthesized logic from which the FPGA boots off during power on.

Linear Technology LTC6912 Preamplifier

The LTC6912 provides two independent inverting amplifiers with programmable gain. The signal in each channel can be amplified with one of 8 gain settings 0, 1, 2, 5, 10, 20, 50 and 100

corresponding to -120 dB, 0 dB, 6 dB, 14 dB, 20 dB, 26 dB, 34 dB and 40 dB. The LTC6912 is programmed by the FPGA using the Synchronous Peripheral Interface (SPI) bus.

Linear Technology LT1568 anti-aliasing filter

The output of the preamplifier is filtered by the LT1568 anti-aliasing filter IC configured as a dual second-order Bessel filter with a cutoff frequency of 11,025 Hz.

Linear Technology LTC1407 A/D converter

The LTC1407 is a stereo A/D converter (ADC) and samples the microphone outputs from the bilateral BTE connected to their respective Freedom coils. The ADC has 1.5 Msps throughput per channel, operates at a sampling frequency of 22,050 Hz and presents a 14-bit two's complement digital output (interleaved left and right channels) to the FPGA. The samples are received by the FPGA over the SPI interface.

Texas Instruments TPS75003 Power Management IC

The TPS75003 is a triple-supply power management IC and supplies power to the FPGA and platform Flash PROM. The TPS75003 takes a 5 V input from the external battery pack and generates 1.2 V for VCCINT (core voltage), 3.3 V for VCCO (I/O voltage) and 2.5 V for VCCAUX (JTAG, Digital Clock Manager and other circuitry). The TPS75003 is a switching regulator (Pulse Width Modulation control) type and is "on" only when power is needed.

For the SPI interfaces above, the FPGA is the bus-master. The FPGA board also has a Lemo mini-coax connector (see Figure 2, labeled Trigger-Out connector) providing access to an output trigger signal. A 5V trigger signal can be generated from the FPGA. This trigger signal can be used for synchronization purposes in external recording systems of evoked potentials. The trigger output signal is not connected directly to the patient; hence it poses no safety concerns. Rather it is used as input to external neural-recording systems (e.g., Neuroscan, Compumedics Ltd), which have been approved by FDA for use with human subjects.

The FPGA board has two Cochlear headset sockets into which plug the two BTE cables shown in Figure 4. Two sockets are used in order to accommodate bilateral cochlear implant recipients. In the case of unilateral recipients (i.e., patients with a single cochlear implant), only one of the two sockets will be used. To ensure that patients will not plug into the FPGA board a commercially available cable, we use a different size socket that does not mate with the commercial cable used previously in body-worn processors. The cable that can plug into this socket is made by Witco of Jupiter Dentsu, Ltd, a company headquartered in Japan. This cable is not commercially available.

An enclosure has been built for the FPGA-interface board and snapshots (taken from multiple angles) of the enclosure are shown in Figure 4.

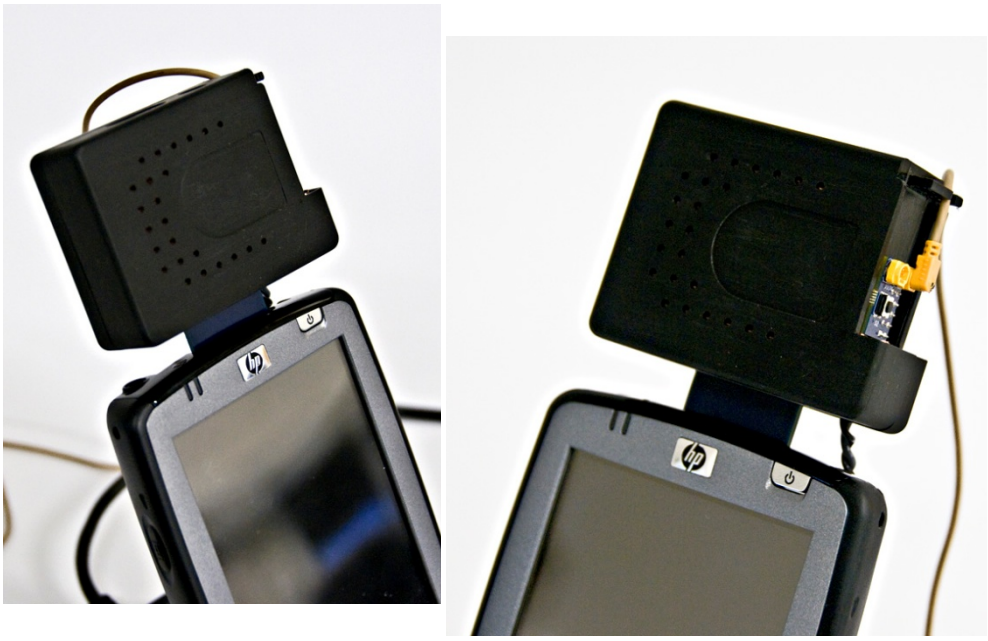

Figure 4. Pictures of the enclosure of the FPGA-interface board taken from two different angles.

The FPGA sends to the Freedom Coil a set of parameters which provide information about the mode of stimulation as well as the current level (amplitude) to be used to stimulate each electrode. This is done using either the embedded protocol (Daly and McDermott, 1998), for the CI24 (and CI24R, CI24RE implants) implant or the expanded protocol (Crosby *et al*., 1985) for the CI22 implant.

2.3 Software Development

Figure 5 shows the organization of the software running on the PDA and FPGA. The software running on the PDA performs the signal processing (i.e., implements the speech coding strategy) while the software running on the FPGA implements the communication protocol needed for proper communication with the Freedom transmission coil. The input to the PDA code is the patient's MAP file along with the signals captured by the left and right microphones. Among other things, the MAP file specifies the stimulation rate, stimulation mode (monopolar, bipolar, etc), pulse width, type of electrode array used and the threshold (T) and most-comfortable (M)

current levels. The block READ PATIENT FILE reads in a patient's file saved in the local directory as ASCII text file and returns a structure containing information about:

- threshold (T) and most-comfortable (M) levels for each electrode
- the sound coding strategy used (CIS-like, ACE-like)
- number and set of active electrodes
- mode of stimulation (e.g., BP+1, MP, etc)
- biphasic stimulus information (phase width, phase gap, pulse period)
- stimulation rate (pulses/sec)
- type of electrode array (e.g., contour)
- implant type (e.g., CI22, CI24, CI24R)

The researchers have the freedom to program any strategy they find appropriate for their research. We make a distinction between CIS –like and ACE-like strategies because different limits are imposed on the stimulation parameters depending on whether the same set of electrodes are stimulated in each cycle (e.g., CIS-like) or a sub-set of electrodes are stimulated in each cycle (e.g., ACE-like). The limits on the stimulation parameters were obtained from Cochlear Corporation**.** The CIS-like and ACE-like options taken together cover all possibilities in terms of the Investigators programming the PDA processor with new signal processing strategies.

The stimulation parameters saved in the patient's file are checked in every cycle prior to stimulation. The error checking is performed on both the PDA and FPGA. Validation tests were conducted to verify that the stimulation parameters are kept within safe limits.

The GET INPUT DATA block (Fig. 5) captures (and buffers) the signal from the microphone(s), located in the BTE(s). The PROCESS DATA block takes as input the patient's MAP file and acquired signal(s) and returns the amplitudes to be transmitted to the cochlear implant via the FPGA. The amplitudes can be obtained either by bandpass filtering the signal into a finite number of bands (e.g., 12, 22) and detecting the envelope in each band, or by computing the FFT spectrum of the signal and estimating the power in each band. The researchers have the freedom to implement their own sound processing strategy. The ERROR CHECKING block takes as input the stimulation parameters along with the envelope amplitudes. The envelope amplitudes are checked against the M levels to ensure that they fall within the electrical dynamic range of each electrode. The user can change dynamically all stimulation parameters, except the M levels. The user can not change the M levels from those originally entered in the patient file. The majority of the information contained in the MAP can be used by researchers to implement new sound processing strategies. Limits, however, are imposed on all MAP parameters. Certain stimulation parameters cannot be modified by the user. For instance, the biphasic pulse width cannot exceed 400 μsecs/phase (in general, the maximum allowable pulse width depends on the stimulation rate). This 400 μsecs/phase upper limit is based on evidence from physiological studies (McCreery *et al*., 1988, 1990; Shannon, 1992). Hence, even if the researcher chooses to modify the contents of the MAP, those changes will be checked to ensure that the electrical

stimulation pattern is safe. The stimulation parameters are checked in each cycle to ensure that they fall within the acceptable and safe limits, and validation tests were conducted to verify this. For safety purposes, the source code of ERROR CHECKING will not be provided to the researchers. In doing so, we ensure that researchers will not program the PDA device with stimulation parameters other than the ones already approved by FDA for the commercial speech processor and the ones tested. If any stimulation parameters are found to fall outside the permissible range, they will be saturated to the maximum allowable value.

Following the ERROR CHECKING block, the SEND DATA block sends the data (envelope amplitudes and stimulation parameters) to the FPGA. The software running on the FPGA prepares the received data for RF transmission using the expanded protocol (Crosby et al., 1985) for the CI22 system and the embedded data protocol (Daly and McDermott, 1998) for the CI24 system. For safety purposes, the source code of SEND DATA and the source code running on the FPGA will not be provided to the researchers.

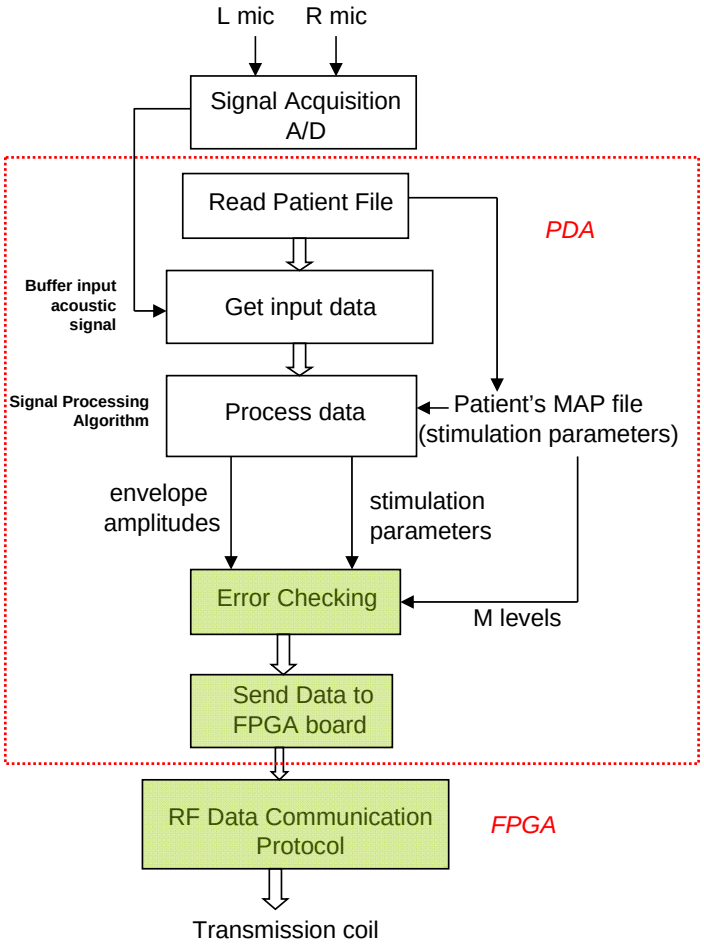

Figure 5. Software Organization. The code running in the blocks shaded in green will not be accessible to the users. Software running on the PDA is shown within the enclosed dashed (red color) rectangle. The software in the filled green-colored blocks is not accessible to the user.

The ERROR CHECKING (Fig. 5) software routine is the gateway routine to electrical stimulation and is thus designed with great caution. This routine takes as input the patient's MAP file and the set of amplitudes (current levels) used for stimulation. From the patient's file, information is extracted about the patient's stimulation parameters. Both the stimulation parameters and amplitude values are checked to ensure that they fall within a permissible range. The permissible range of stimulation parameters was taken from Cochlear Corporation's documents.

A. Checking for valid range of envelope amplitudes

The envelope amplitudes of each electrode need to be limited within the range of threshold (T) to most comfortable (M) levels (the T and M levels are expressed in clinical units and can range from 0 to 255). Most importantly, the envelope amplitude of each active electrode is checked to ensure that it is smaller than the M level of each electrode. If any of the amplitudes falls outside this range, the program saturates the amplitude to the corresponding M level. This is done to avoid overstimulation. The M levels can be obtained using the clinical fitting software, *Custom Sound (v.2)*, and are subsequently entered into the patient's file. As mentioned previously, the researchers are not allowed to change dynamically (i.e., during stimulation and at each cycle) the M levels from those originally entered in the patient file. This is done as an additional measure to ensure that any change in M levels would not cause overstimulation.

For the CI24 and Freedom implants (CI24RE) that use the contour electrode array, further safety checks are set in place to limit the charge density. More specifically, the maximum stimulation level allowed depends on the pulse width, from which a maximum charge-density level (CDM) is computed. The envelope amplitude is thus not allowed to exceed the minimum of the M and CDM levels.

B. Checking for valid range of stimulation parameters

The relationship between the various stimulation parameters available is complex and it depends among other things on: (1) the generation of the Nucleus device (e.g., CI22, CI24), (2) the electrode array used and (3) the stimulation strategy used (CIS-like vs. ACE-like). For instance, the allowable pulse width depends on both the stimulation strategy used and the generation of the Nucleus device. Similarly, the stimulation rate is limited by the hardware of the Nucleus device, with only low rates (e.g., 250 pps) being allowed (and possible) in the CI22 device and highest rates being possible in the latest CI24RE device.

The above relationships and dependencies among stimulation parameters were taken into account when writing and testing the ERROR CHECKING routine. Provisions were made for the above dependencies and more precisely about:

I. Valid stimulation modes

The different modes of stimulation available in the CI22 and CI24 devices are considered and checked for conformity. These include the monopolar, bipolar (e.g., BP+2) and common ground stimulation modes.

II. Pulse-rate and pulse width dependency

The maximum pulse width allowed depends on: (1) the stimulation rate and (2) strategy used (CIS-like vs. ACE-like). The maximum pulse width allowed never exceeds 400 μs/phase. The maximum stimulation rate allowed depends on the generation of the Nucleus device. The Freedom device (CI24RE), for instance, allows for a maximum stimulation rate of 32,000 pulses/sec (aggregate rate).

III. Charge density limitations for different electrode arrays

For the CI24 and Freedom implants (CI24RE) which use the contour electrode array, there are amplitude/pulse width combinations that may result in charge and charge density values outside the estimated safe limits. The maximum charge-density level (CHD) allowed depends on the pulse width. The envelope amplitudes are not allowed to exceed the CHD level. In contrast, no such limitations are imposed on implants with soft electrode arrays. In this case, the envelope amplitudes are not allowed to exceed the M levels.

If any of the parameter values falls outside the allowable range, the program limits (saturates) their values to the permissible range.

3. Recording cortical auditory evoked potentials

The PDA has the capability of recording EEG and cortical auditory evoked potentials (CAEPs) – see Quarterly Progress Reports (QPR) 2, 4 and 5. More precisely, the Dataq-CF2 or the CF-6004 data acquisition cards can be used to record CAEPs or EEG. Both cards plug into the compact flash slot of the PDA. The Dataq-CF2 card (C-Cubed Ltd, UK) has four 24-bit analog input lines, two 12-bit analog output lines and four digital I/O channels. It supports sampling rates up to 40 kHz (see QPR 2). The CF-6004 compact flash card is manufactured by National Instruments (NI) and can be programmed in LabVIEW (see QPRs 4 and 5).

Given the limited number (4) of recording channels provided by the above two compact-flash cards, we decided to provide access to a trigger signal in the FPGA board. The FPGA board is equipped with a Lemo mini-coax connector (see Figure 2, labeled Trigger-Out connector) providing access to an output trigger signal. A 5V trigger signal can be generated from the FPGA. This trigger signal can be used for synchronization purposes in external recording systems of evoked potentials. The trigger output signal is not connected directly to the patient; hence it poses no safety concerns. Rather it is used as input to external neural-recording systems (e.g., Neuroscan, Compumedics Ltd), which have been approved by FDA for use with human subjects.

4. Animal Stimulators

4.1. Bench-top Stimulator: System Overview & Methodology

The bench top, bipolar stimulator or BT-BiSTM is a multichannel bipolar current source designed for acute experiments on percutaneous, animal cochlear implant systems. Created originally as the precursor to the portable version of the stimulation system, the BT-BiSTM offers researchers the ability to study the effects of channel interactions on speech recognition particularly as a function of the electrode array configuration. While the BT-BiSTM is intended to be used primarily for bipolar stimulation, it is also capable of generating up to eight independent, time interleaved monopolar signals. Therefore, studies on the effects of time interleaved monopolar stimulation on speech perception can also be made with use of this device.

The BT-BiSTM is a highly versatile platform capable of generating up to 8 simultaneous channels over a wide array of excitation patterns including both pulsatile and analogue-like, or combinations of both. Built around a 9-bit configurable current source chip, the BT-BiSTM platform possesses the following specifications:

- 8 independently controlled bipolar channels or up to 8 independently controlled time interleaved monopolar channels, each electrically isolated and charge-balanced
- 5V compliance voltage
- 1mA maximum current amplitude per channel
- 9-bit current amplitude resolution per channel (1.95 µA)
- 4µs minimum pulse width per channel (1 sec maximum pulse width)
- 0µs minimum interphase gap per channel (maximum allowed interphase gap depends on maximum pulse width)
- 4µs minimum interstimulus interval per channel (maximum depends on desired pulse rate)
- 83.3kHz maximum pulse rate per channel
- >50MΩ output resistance per channel

With this platform, a wide array of stimulation techniques for cochlear implants can be tested on animals. By varying parameters such as current amplitude, pulse width, interphase gap, inter-stimulus interval (ISI) and pulse rate, a multitude of stimulation patterns can be created both in phase (simultaneous) or interleaved across multiple channels.

Depending upon the demands of particular applications, the BT-BiSTM is capable of generating up to eight independently controlled and highly complex bipolar signals each varying in pulse width, interphase gap, pulse rate and current amplitude. A portion of the output channels can be generated simultaneously in phase while others can be interleaved in time. The time duration of a single cycle of such complex stimulation patterns (multiple cycles can continuously be generated in a periodic fashion for extended periods of time) is a function of the shortest non-zero time constraint of the waveform -typically the interphase gap. For instance, if the

minimum required interphase gap of a channel output is 2µs then the output sampling rate of the bipolar stimulator chip, that is the rate at which a single analog current output sample can be generated by the onboard current stimulator chip, must be chosen sufficiently high in order to maintain an adequate time resolution for the specified interphase gap. Chosen as such is an output sampling rate of 0.1µs which corresponds to 12.8s of a single stimulation pattern for all 8 channels that can be stored in memory and then continuously regenerated in a loop-like fashion over extended periods of time. For applications with looser time constraints that can be met with slower output sampling rates, even lengthier stimulation patterns can be stored and generated.

In addition to the 8-channel current source BT-BiSTM board shown in Fig. 6, the software needed to control the board is also available in an easy to use and user-friendly graphical user interface (GUI) built on top of the National Instruments (NI) graphical programming environment, LabVIEW. When combined with NI's 32 channel, high speed digital output board, the PCI-6534[1], which serves as the hardware control interface between any PC equipped with a standard PCI slot and the BT-BiSTM board, the BT-BiSTM GUI greatly simplifies the task of using the board in order to output a desired set of electrical stimulation patterns by eliminating the need of users to program the board. Note that the PCI-6534 card supports up to a 20-MHz clock rate, but for our experiments and testing we used a 10-MHz clock rate. Waveform parameters such as pulse rate or pulse width may simply be entered into the GUI for a desired set of stimuli without knowledge of the underlying sequence of digital control signals needed to control the BT-BiSTM board, thus reducing the time required in learning how to use the platform thus allowing researchers to focus their efforts on conducting animal experiments.

4.2 BT-BiSTM Hardware Architecture

Shown in Fig. 6 is a photograph of the BT-BiSTM board. At the core of the board is the 9-bit configurable current source chip, simply referred to as the BiSTM chip. The BiSTM chip is designed to provide programmable anodic and cathodic current pulses for stimulation. By using a dynamic biasing scheme, the stimulator can realize 9 bits of resolution with a single 7-bit binary-weighted digital to analog converter (DAC). Hence, good linearity and a small implementation silicon area are achieved simultaneously. Moreover, active cascade output stages are used in the BiSTM chip to achieve high output impedance. Output impedance is further improved with the use of stacking MOS structures which can minimize hot-carrier effects and maintain output current accuracy through large voltage compliance.

[1] http://sine.ni.com/nips/cds/view/p/lang/en/nid/13505

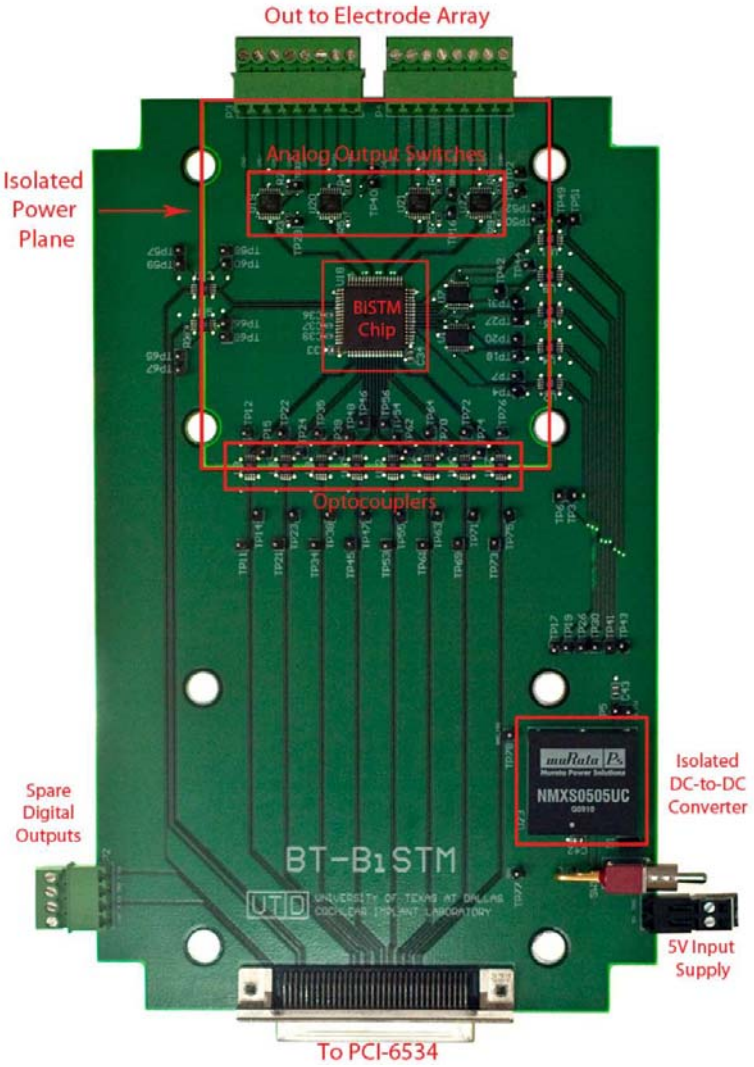

Figure 6: BT-BiSTM 8-channel bipolar stimulator board.

Each of the board's 8 bipolar outputs is electrically isolated from the line power supplying the board in order to avoid problems incurred by ground loops and voltage spikes. Electrical isolation is achieved with use of the NMXS0505UC isolated DC-to-DC converter made by Murata and the IL711 optocoupler manufactured by Nonvolatile Electronics (NVE).

The NMXS0505UC divides the 5V input supply voltage into two separate power/ground planes: 1) tied to line power or that of the electrical circuit within a building and 2) one apart from line power, having no direct electrical connection to the 5V input supply. Once sufficiently isolated, the BiSTM current output signals no longer share a common reference with any other electrical equipment which may be attached to a test animal such as neural recording systems, thereby eliminating the formation of potential ground loops between various devices and further eliminating the risk of physically harming the animal or incurring distortions associated with electrical artifacts during recordings. In addition to the electrical isolation through the BT-BiSTM power supply circuit provided by the NMXS0505UC, the Murata IL711 optocouplers further

isolate the 30 digital control signals entering the 68-pin Dsub connector at the base of the circuit board. Thus, all sources of electricity attached to the board, both for power and control, are isolated from the outputs of the BiSTM chip.

The BiSTM chip has at each of its 8 bipolar outputs a constant compliance voltage of 5V when actively generating a signal or when at rest with no current flow. Depending upon the application, the 5V found at each of the 8 bipolar outputs of the chip may be either disconnected or left attached from the output connectors located on the top of the board when in rest, and of course, attached when active. Achieved by passing each of the 8 BiSTM outputs through an electronically controlled single-pole-single-throw (SPST) switch, the 5V compliance voltage may be applied or removed from the implanted electrode array as needed.

Also available on the BT-BiSTM board are 2 spare digital control signals. Chosen to control the BT-BiSTM board is the PCI-6534 made by NI. Equipped with 32 high-speed digital output signals, two of the PCI-6534 outputs are unused and routed out to the left-most connector of the board where it is available to users if needed.

Attached through a cable to the 68-pin Dsub connector located at the base of the BT-BiSTM board is the PCI-6534 digital output card shown in Fig. 7. The PCI-6534 is equipped with 32 high speed digital output signals which serve as the input control signals to the BT-BiSTM board (though only 30 are needed) where each channel has a maximum data rate of 20 Mbits/s. To ensure accurate generation of waveform stimuli, all the necessary control signals for a given set of stimulation parameters are first stored onto the PCI6534 64 MBytes of onboard memory and then transmitted to the BT-BiSTM in a repeated pattern at a data rate based upon the onboard 20 MHz clock. Doing so guarantees that the desired timing parameters such as pulse width or inter-stimulus interval are maintained at the outputs with high precision.

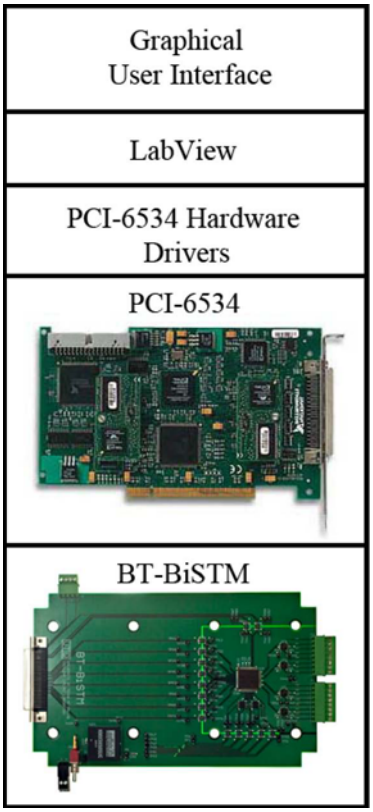

Figure 7: BT-BiSTM stimulation platform control stack.

A LabVIEW GUI has been created to simplify the task of controlling the BT-BiSTM board by allowing the user to simply specify a set of desired stimulation parameters, without concern of how the underlying 30 digital control signals function to control the board. Essentially, the user is only required to learn how to use the LabVIEW GUI with only minimal knowledge of how the lower levels of the control stack operate (Fig. 8). Fig. 8 shows a snapshot of the LabVIEW GUI. As can be seen, the user can easily change the stimulation rate, the pulse width, pulse amplitude and can also select individual channels to be stimulated simultaneously, interleaved or combinations thereof.

The PCI 6534 card can be controlled using the NI-DAQmx driver. This driver provides a number of optimized application programming interfaces (APIs) for configuring the channels, setting up the buffers and performing acquisition. In the Windows environment, these APIs can be called from LabVIEW or .NET languages such as Microsoft Visual C or Microsoft Visual Basic. The developed GUI in LabVIEW uses the subVIs provided by the DAQmx toolbox to configure the 32bit digital channels and to set a data transfer rate based upon the board's internal clock. DAQmx can also be used to initialize the buffers within the onboard memory which helps to achieve a higher output rate independent of the PCI bus bandwidth.

Additionally, if needed, users are able to create custom applications that control the BT-BiSTM board in programming environments other than Lab-VIEW. By using the C/C++ library of hardware drivers provided with the PCI-6534 and the BiSTM User's Guide, which describes in

full detail the function of each of the chip's 30 control signals (available upon request), users may create custom applications to control the board in order to better integrate it into their existing test setups.

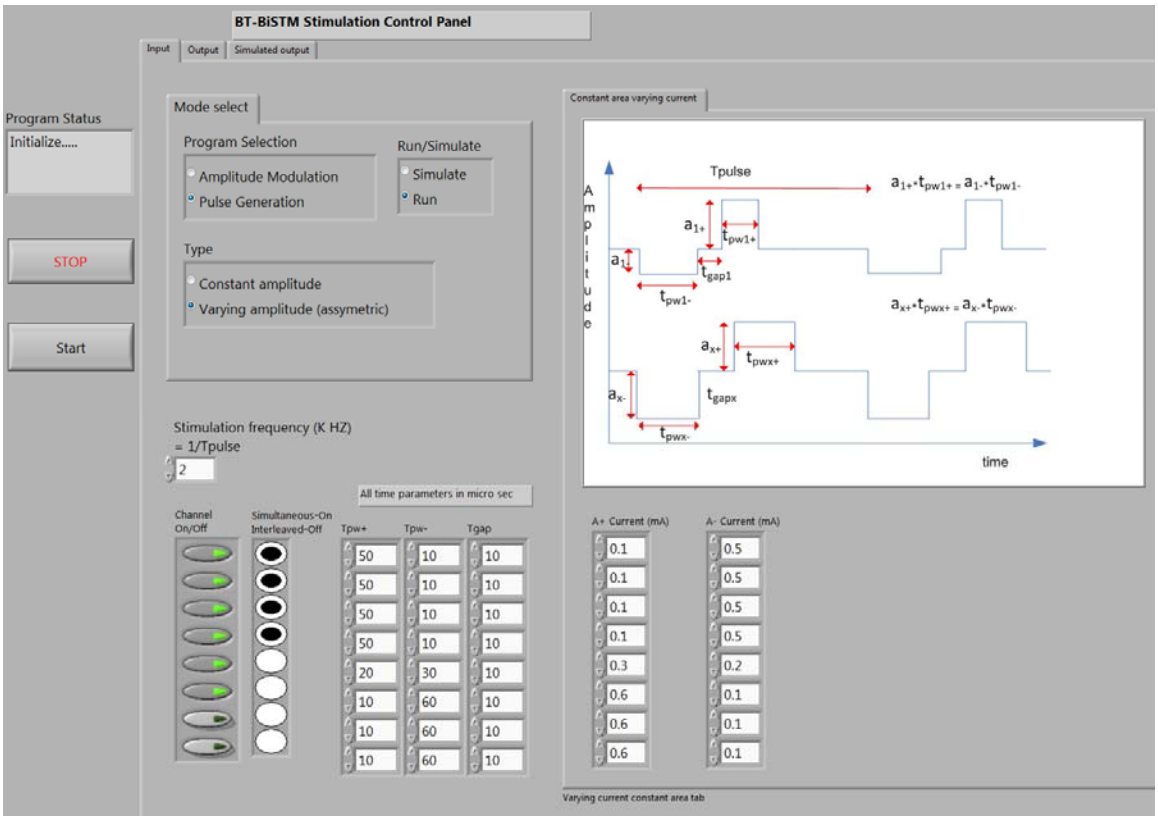

Figure 8: LabVIEW GUI used for specifying and changing stimulation parameters.

For users who prefer Matlab, .m file scripts that control the PCI-6534 are also available. These scripts like those of the LabVIEW GUI eliminate the complexities associated with programming the PCI-6534 in order to generate a specified set of current stimuli. Users are simply required to specify stimulation parameters familiar to them such as current amplitude, pulse width, interphase gap, pulse rate, etc. The .m file script then automatically translates these parameters into the appropriate set of digital control signals generated by the PCI-6534 that in turn drives the current outputs of the BT-BiSTM board. The PCI-6534 Matlab scripts can also be easily integrated into existing test control software also written in the Matlab programming environment. Therefore, coordination of a whole host of devices needed in an experiment, ranging from recording instruments and scopes to current stimulators and audio outputs can be realized in a single programming environment.

Lastly, by taking advantage of the BT-BiSTM open control interface, digital output boards other than the PCI-6534 may also be used to control the BT-BiSTM given that these boards have a

minimum of 30 outputs, each 5V TTL compatible, and are capable of meeting the timing requirements of a particular application.

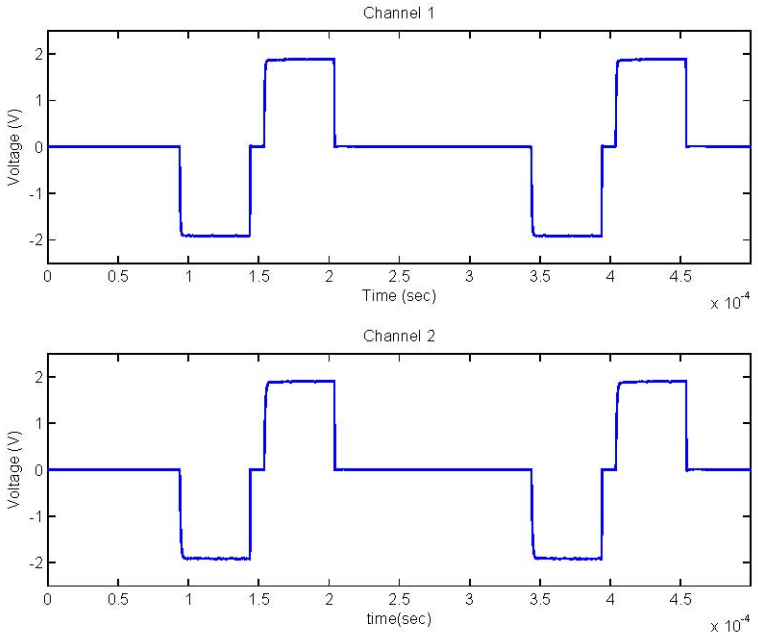

Figure 9: Pulsatile simultaneous stimulation measured over 2kΩ loads.

Sample waveforms are provided in Figs. 9-10 as examples of the BT-BiSTM capabilities. Beginning with the two simultaneous charge-balanced bipolar signals shown in Fig. 9 where channels 1 and 2 generate identical signals locked in phase with pulse widths of 50µs, interphase gaps of 10µs, inter-stimulus interval of 140µs, and current amplitudes of 965µA. Measurements are taken over 2kΩ loads. Note, that although only 2 channels are displayed in this example, the BT-BiSTM is capable of generating simultaneous signals over all 8 channels.

To further demonstrate the BT-BiSTM's ability to generate nearly any arbitrary waveform pattern, two additional phase locked signals are shown in Fig. 10 where channel 2 generates a symmetric bipolar signal and channel 1 generates an asymmetric bipolar signal. For both outputs, the total charge (defined as the time integral of the absolute value of the pulse voltage while active) over the cathodic pulses are equal in voltage (current) and pulse width where 765µA is applied to both channels for 10µs. However, for the anodic pulses, channel 2 (as it does for its cathodic pulses) outputs 765µA for 10µs whereas channel 1 outputs 191µA for 40µs. Measurements are taken over 2kΩ loads.

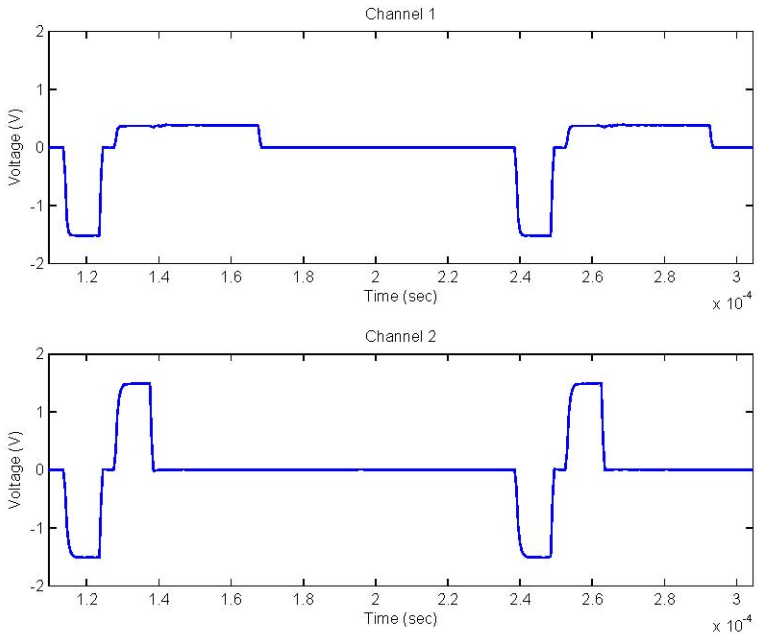

Figure 10: Symmetric/asymmetric simultaneous stimulation measured over 2kΩ loads.

As a demonstration of the BT-BiSTM's ability to also generate amplitude modulated (AM) signals, displayed in Fig. 11 are three sets of phase locked waveforms. In Fig. 11, the frequency, f, of the low-frequency envelope for channels 1 and 2 is equal to 400Hz and 200Hz, respectively. For both channels, the bipolar carrier signal has a pulse width of 50µs, interphase gap of 10µs, and inter-stimulus interval of 140µs. Plots are shown for modulation depths of 25%, 50% and 100%.

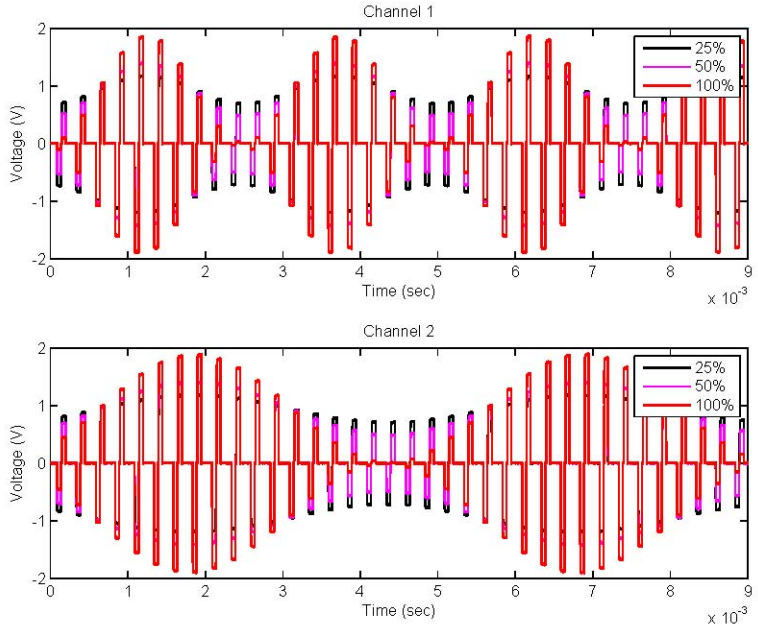

Figure 11: Simultaneous amplitude modulation stimulation measured over 2kΩ loads.

4.3. Portable Stimulator: SDIO-BiSTM System Overview

A portable adaptation of the bipolar stimulation platform was built, referred to as the SDIO-BiSTM. Similar to the open-interface research platform, the SDIO-BiSTM exploits the mobile processing capabilities of a personal digital assistant (PDA) and combines it with a custom made interface card that communicates with the PDA through a secure digital IO (SDIO) slot, hence the SDIO prefix in the name of the portable stimulation platform. In the case of the SDIO-BiSTM, the interface board consists primarily of the BiSTM chip.

The SDIO-BiSTM is comprised of a main board and a daughter board as shown in Figures 12 and 13, respectively. Listed below are the main circuit elements of the main board and their respective functions.

- Xilinx Spartan FPGA: Accepts desired output waveform parameters from a GUI application running on the PDA and controls the BiSTM chip accordingly in a way similar to that of the PCI-6534 in the case of the BT-BiSTM platform.
- Arasan SDIO interface controller: Controls communication between the PDA and FPGA.
- 80-pin board-to-board connector: Routes various control/power signals to the BiSTM chip located on the daughter board.
- Miscellaneous power circuitry: Converts 6V of battery supply power to the various voltage levels needed to power the board.

The daughter board circuit elements and respective functions are as follows:

- BiSTM chip: 8 channel configurable bipolar current source.
- Analog output switches: Disconnects the 5V compliance voltage from the test subject when the BiSTM chip is in reset.
- 5V low drop-out regulator (LDO): Converts/regulates 6V battery power down to the 5V BiSTM chip supply power.
- Voltage level shifters: Translates the FPGA's 3.3V digital signal to the required 5V level of the BiSTM chip.
- 16-pin output connector: Routes the 8 bipolar signals to the implanted cochlear electrode array.

The SDIO-BiSTM board design was divided into two separate boards in order to minimize the overall size of the board. Combining both boards into a single board would have been many times larger and impractical. Also note that since the SDIO-BiSTM board operates on battery power to facilitate mobility; the 8 BiSTM bipolar outputs are electrically isolated from any other electrical devices that may be attached to the test animal. The experimenter has additional access to grounds on the board that can be easily connected to a corresponding sensing ground or extra-cochlear electrode ground. DC-blocking capacitors (1 μF) are placed in series to the

bipolar outputs to remove any residual current. Tests of SDIO-BiSTM platform have been conducted in which biphasic pulses were generated to test the operation of the SDIO-BiSTM daughter card. The control logic for the stimulation was coded in Verilog and synthesized for the XC3S1500 FPGA under Xilinx ISE 11.1 Project Navigator.

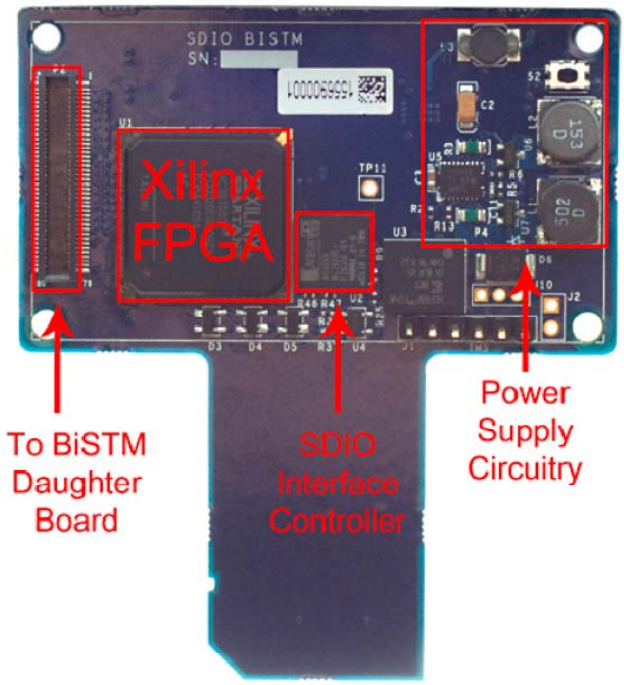

Figure 12: SDIO-BiSTM main board prototype.

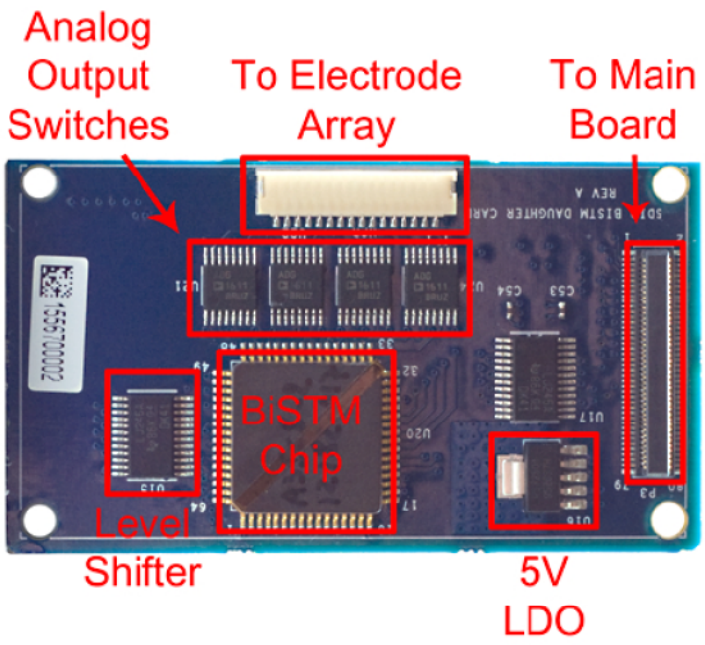

Figure 13: SDIO-BiSTM daughter board prototype.

Fig. 14 shows the BiSTM chip control signals in the lower half of the oscilloscope display. Shown in the upper half of the oscilloscope display are the resulting biphasic pulses measured across the output of channel 8 (measurements taken across a 2.2kΩ resistor). The current amplitude level bits, b1-b5, are also shown. The measurement was taken using two analog channel probes with one of the probes connected between the positive output terminal and ground and the second probe connected between the negative output and ground and taking the arithmetic difference between the two analog channels.

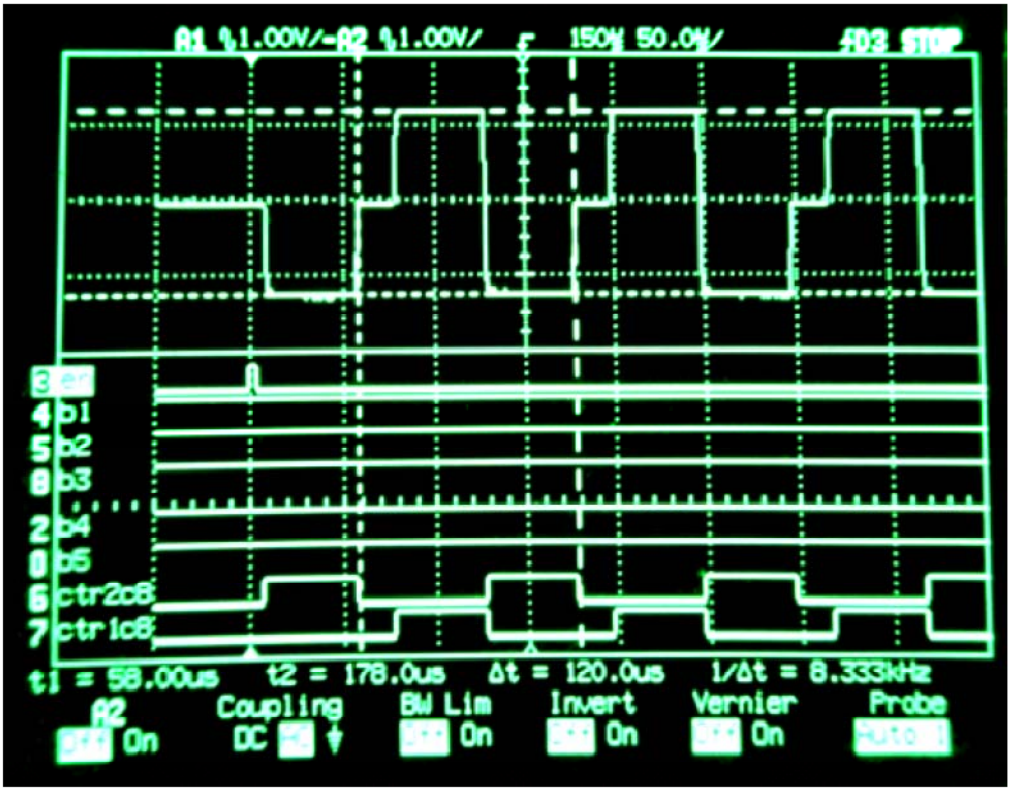

Figure 14: SDIO-BiSTM sample output waveform generation.

As can be seen, to generate the negative half of the pulse the CTRL1 CH8 control signal is set to 0 and the CTLR2 CH8 control signal is varied to either 0 or 1 in a pattern that resembles the desired output waveform where the output current is turned on when CTRL2 CH8 is in the ON state and turned off when CTRL2 CH8 is in the OFF state. To generate the positive half of the pulse the roles of CTRL1 CH8 and CTRL2 CH8 as described above is reversed. To generate the interphase gap both CTRL1 CH8 and CTRL2 CH8 are set to 0.

Because the SDIO-BiSTM was designed as a portable stimulator for chronic animal studies, the physical dimensions and weight of the overall system including the PDA, the current stimulation board, and battery pack have been minimized to the extent possible. Depending upon the animal to which the device will be used, the following physical specifications should facilitate portability.

- Dimensions of overall system: 6 x 3 x 0.6 inches
- Weight of overall system: 0.66 pounds

Furthermore, in order to minimize the frequency at which batteries must be replaced and recharged, preliminary tests have shown that the battery life of the overall system is

approximately 4 hours. Multiple spare batteries are available with the system. Depleted batteries can quickly be replaced with those fully charged and allowed to be recharged amongst a set of other spare batteries.

4.4. Monopolar Bench-Top Stimulator

A monopolar stimulator, referred to as the BT-MoSTM, was also built. The new stimulator board is designed around two dual monopolar stimulator chips that feature 8 monopolar channels per chip for a total of 16 charge-balanced monopolar channels, each sharing a common reference and capable of sourcing a maximum of 1mA. The 16 channels can be independently controlled, each varying in stimulation parameters including current amplitude, pulse width, interphase gap, pulse rate, etc. Much like the BT-BiSTM board, the new monopolar version of the board is also capable of generating a vast array of varying pulsitile and analogue-like stimulation patterns in either simultaneous or interleaved modes or combinations thereof. A user-friendly and intuitive LabVIEW GUI as well as Matlab scripts is available with the BT-MoSTM board to simplify its use and control in order to minimize the time required by researchers to become familiar with the system. An image of the BT-MoSTM board is shown in Fig. 15.

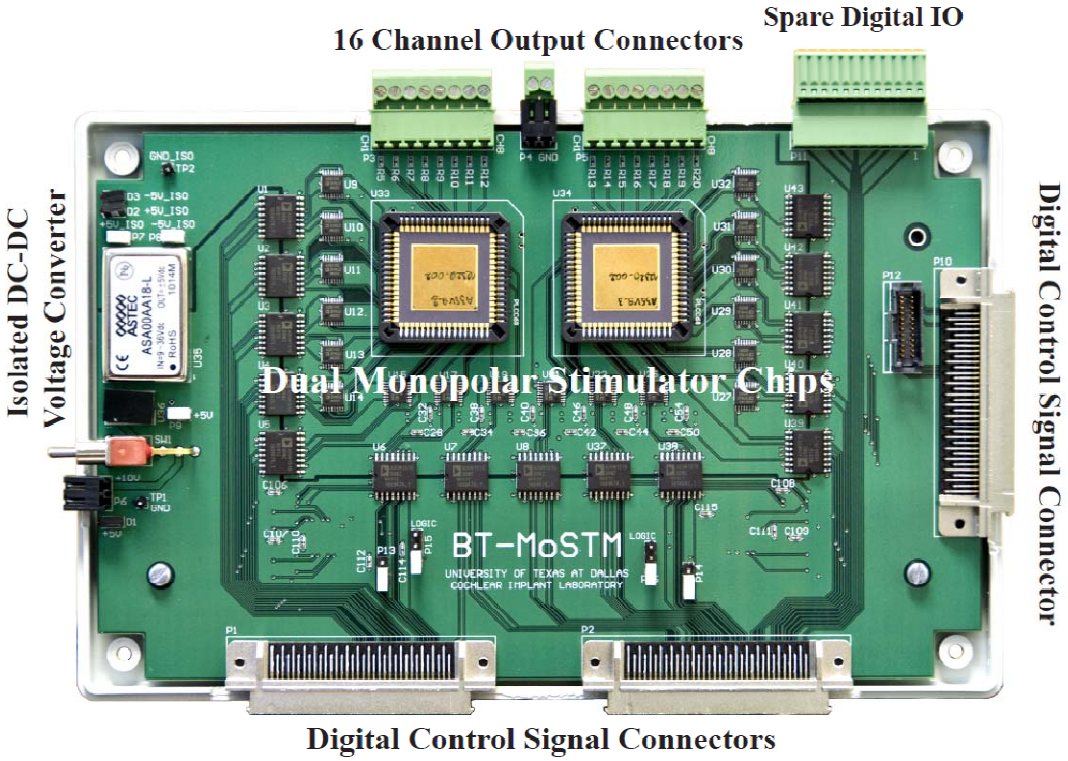

Figure 15: SDIO-MoSTM benchtop stimulator.

5.0 IDE Application

An IDE application has been submitted to FDA for the PDA speech processor. Extensive software validation experiments have been done to ensure that safety checks are in place. The data from these tests have been submitted to FDA in support of our IDE application. In addition, electromagnetic interference tests have been conducted. Current FCC and FDA regulations require that class B medical devices meet specified maximum levels for both radiated and conducted electromagnetic interference (EMI). Radiated EMI covers the frequency range from 30 MHz to 1.0 GHz. EMI arises due to the transfer of energy from one source conducting RF currents to other radiating or conducting elements such as cables or power cords. The PDA processor has been sent to Southwest Research Institute, San Antonio, TX for EMI testing, and specifically for compliance to the applicable emission and immunity requirements of IEC 60601-1-2. The PDA processor has also been sent to OMEDtech, Edmond, OK for environmental testing to assess the effects of environmental conditions such as temperature and humidity. All testing was done according to the following standards: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-20 and IEC 60068-2-61. The testing has been completed and the PDA processor has been found to be compliant to all requirements specified in the above IEC standards. The IDE application has been approved by FDA in May 2011.

6.0 Distribution to Research Centers

As required by the contract, the PDA speech processors were delivered to multiple research centers across the US. After consultation with NIDCD-NIH program Director, Dr. Roger Miller, the following 8 investigators were chosen:

1. Dr. Jay Rubinstein, University of Washington, WA
2. Dr. Michael Dorman/Chris Brown, Arizona State University, AZ
3. Dr. Ruth Litovsky, Univ. of Wisconsin-Madison, WI
4. Dr. Q. Fu/R. Shannon, House Ear Institute, Los Angeles, CA
5. Dr. Mario Svirsky, NYU, New York, NY.
6. Dr. Leslie Collins, Duke University
7. Dr. Bom Jun Kwon, Ohio State University, OH
8. Dr. Fan-Gang Zeng, UC-Irvine, CA

A PDA processor has also been delivered to Dr. James Phillips (University of Washington, WA) lab for vestibular prosthesis studies in non-human primates.

A workshop was held in Dec 2010 to provide training to the above investigators on the safe use of the PDA processor. A follow-up meeting was conducted at the ARO conference in Feb 2011, and another meeting is scheduled for the CIAP meeting in July 2011.

The animal (bench-top) stimulators have been delivered to:

1. Dr. Xiaoqin Wang, Johns Hopkins University, Maryland, MD
2. Dr. John Middlebrooks, Univ. of California, Irvine, CA
3. Dr. Robert Shepherd, Bionic Ear Institute, Australia
4. Dr. Sat Panu, Lawrence Livermore National Laboratory, Livermore, CA
5. Dr. Bertrand Delgutte, RLE/MIT, MEEI, Boston, MA

At Dr. Wang's lab, the BT-BiSTM board has been used in chronic neurophysiological experiments in awake marmosets. Plans are underway to deliver portable stimulators to the above investigators.

REFERENCES

Crosby, P., Daly, C., Money, D., Patrick, J., Seligman, M. and Kuzma, J. (1985). "Cochlear implant system for an auditory prosthesis," *US Patent* 4,532,930.

Daly, C. and McDermott, H. (1998). "Embedded data link and protocol," *US Patent* 5,741,314.

Loizou, P. (1998) "Mimicking the human ear," *IEEE Signal Processing Magazine,* 15, 101-130.

McCreery, D., Agnew, W., Yuen, T. and Bullara, L. (1988). "Comparison of neural damage induced by electrical stimulation with faradic and capacitor electrodes," *Ann. Biomed*. Eng., 16, 463-481.

McCreery, D., Agnew, W., Yuen, T. and Bullara, L. (1990). "Charge density and charge per phase as cofactors in neural injury induced by electrical stimulation," *IEEE Trans. Biomed. Eng*, BME-37, 996-1001.

Shannon, R. (1992). "A model of safe levels for electrical stimulation," *IEEE Trans. Biomed. Eng*., 39(4), 424-426.

Vandali, A. E., Whitford, L. A., Plant, K. L. and Clark, G. M. (2000). "Speech perception as a function of electrical stimulation rate using the Nucleus 24 Cochlear Implant System," *Ear Hear.*, *21*, 608–624.