Metrology Challenges for Emerging Devices and Materials

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The Erik Jonsson School of Engineering and Computer Science
- $200M from state of Texas
- $100M in Private and Corporate Support
- Deliverables
  - 40 New Faculty for the Engineering School
  - 200,000 sq. ft. Research Facility
  - Additional Departments & Degree Programs
    • MS & PhD in Materials Science and Engineering
    • BS in Computer Engineering
    • BS/MS/PhD in Bioengineering
  - 50 PhD's per Year
  - $30M to $50M per Year in External Research Funding
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Recent micro-/nano- electronics faculty

- **B. Gnade**
  Electronic materials, organic electronics

- **B. Wallace**
  Advanced materials for device scaling

- **M. Kim**
  Advanced analytical characterization

- **W. Hu**
  Nanolithography

- **J. Y. Kim**
  ALD and nanoscale materials

- **E. Vogel**
  Device fabrication and characterization

- **K. J. Cho**
  Nanoscale computation
New Science and Engineering Research Building

New cleanroom with new fab equipment

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New Cluster Tool for Materials Research

Numerous other facilities:
- 2 New high-resolution JEOL TEM/STEM.
- New FEI NOVA FIB/SEM
- New XRD
- New electrical characterization facilities (cascade probe station, parameter analyzers, LCR meters, etc.)
- Wafer bonding cluster tool

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Ken David, “Intel Makes Transistor Breakthrough Using New Materials”,
• Emerging devices and materials

• Metrology challenges
  1. Dimension
  2. Physical structure
  3. Composition
  4. Electronic structure
  5. Within the device of interest

• Emerging architectures

• Conclusions
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Emerging Devices and Materials

**Bulk CMOS**

**Silicon-on-insulator**

**Surround-gate**

![Diagram of Emerging Devices and Materials](image)
Non-Silicon Substrates
- Silicon germanium
- Germanium
- $\text{In}_x\text{Ga}_{1-x}\text{As}$
- InSb

High-k Gate Dielectrics

Metal Gate Electrodes

<table>
<thead>
<tr>
<th>Work Functions</th>
<th>For nMOS</th>
<th>Threshold voltage ±0.5V larger than poly-Si!</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\text{W}:4.1\text{-}5.2$</td>
<td>$\text{Mo}:4.3\text{-}4.6$</td>
<td>$\text{Cr}:4.5\text{-}4.6$</td>
</tr>
<tr>
<td>$\text{Os}:4.7\text{-}4.83$</td>
<td>$\text{Re}:4.6\text{-}4.71$</td>
<td>$\text{Am}:4.52\text{-}4.77$</td>
</tr>
<tr>
<td>$\text{Pt}:4.8\text{-}5.23$</td>
<td>$\text{Ni}:4.5\text{-}5.3$</td>
<td>$\text{WN}<em>{x}\text{TiN}</em>{y}$ $\text{AlN}:4.2\text{-}5.0$</td>
</tr>
</tbody>
</table>

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## Table 4. Emerging Logic Devices

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>RESONANT TUNNELING DIODE – FET</th>
<th>SINGLE ELECTRON TRANSISTOR</th>
<th>RAPID SINGLE QUANTUM FLUX LOGIC</th>
<th>QUANTUM CELLULAR AUTOMATA</th>
<th>NANOTUBE DEVICES</th>
<th>MOLECULAR DEVICES</th>
</tr>
</thead>
<tbody>
<tr>
<td>TYPES</td>
<td>3-Terminal</td>
<td>3-Terminal</td>
<td>Josephson Junction +Inductance Loop</td>
<td>-Electronical QCA -Magnetic QCA</td>
<td>FET</td>
<td>2-Terminal and 3-Terminal</td>
</tr>
<tr>
<td>ADVANTAGES</td>
<td>Density, Performance, RF</td>
<td>Density, Power, Function</td>
<td>High Speed, Potentially Robust, (Insensitive to Timing Error)</td>
<td>High Functional Density, No Interconnect in Signal Path, Fast and Low Power</td>
<td>Density, Power</td>
<td>Identity of Individual Switches i.e., Size, Properties on Sub-nm Level, Potential Solution to Interconnect Problem</td>
</tr>
<tr>
<td>CHALLENGES</td>
<td>Matching of Device Properties Across Water</td>
<td>New Device and System Dimensional Control i.e., Room Temp Operation, Noise Offset Charge, Lack of Drive Current</td>
<td>Limited Fan Out, Dimensional Control (Room Temperature Operation), Architecture, Feedback from Devices, Background Charge</td>
<td>New Device and System, Difficult Route for Fabricating Complex Circuitry</td>
<td></td>
<td>The Erik Jonsson School of Engineering and Computer Science</td>
</tr>
</tbody>
</table>
Emerging Devices and Materials

Beyond CMOS

Confined Devices
NWs, nanotubes, QDs

Molecular Devices

Spin and Ferro Devices


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By 2010 (45 nm node), the transistor physical gate length will be 18 nm and inline, nondestructive microscopy (CD SEM) resolution will need to be 0.16 nm. Test structures and correlation with other techniques (e.g. AFM) are required.

M. Cresswell, T. Vorburger, J. Dagata, R. Dixson, M. Postek (NIST)

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The thickness of the silicon oxynitride gate dielectric is ~1.2 nm today [1].
This is an extreme challenge to physical [2] and electrical [3, 4, 5] metrology.

Confining the dimensionality of silicon improves short channel effects and reduces the need to scale the oxide thickness.

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3D Structure Matters!


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• Need to profile local structural, chemical, and electronic properties.

• Need to deconvolve the true tip geometry from the measurement of the sample.

• The measured size of quantum dots determined using AFM is larger than that determined using TEM.

• It is many times assumed that the quantum dots are perfectly spherical.

• These results indicate that the silicon dots are not perfectly spherical.

Plasmon tomography measurements of silicon quantum dots in SiO₂, courtesy of Aycan Yurtserver and Prof. David Muller, Cornell University.

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By 2010 (45 nm node), dopant distribution must be characterized with 3 nm spatial resolution and 4% accuracy.

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Using geometrically controlled test structures, an increase in effective mobility with decreasing nanowire dimension has been observed.

Numerical results by Zhong have suggested that doping of an outer shell of a silicon nanowire while keeping the core of the nanowire unperturbed may result in an increase in the electron mobility (in contrast to bulk silicon).

There are currently no techniques capable of mapping the composition of nanowires at the spatial resolutions necessary to experimentally verify this result.

Number of Atoms vs. Size
U3O8 Spheres

- Comfort zone for most analytical laboratories
- Current research
- New technology needed

Increasing Sensitivity

Increasing Spatial Resolution

J.-H. Scott (NIST)
Reliability measurements suggest:
- Thinner HfO$_2$ films have less charge trapping and associated instabilities.
- The defects are in the HfO$_2$.
- The energy of the defect is near the edge of the HfO$_2$ conduction band.
A wide variety of analytical characterization (e.g. spectroscopic ellipsometry) is necessary to elucidate the chemical and electronic structure of high-k dielectrics.

Electronic defects are reflected by an adsorption feature 0.2-0.3 eV below the optical bandgap.

These features may be due to localized d-states in nano-crystalline, but not amorphous, materials.

• A small defect density is observed near the interface which increases and then becomes approximately constant.
• The increase may be attributed to the interface between SiO₂ and HfO₂.

• Charge pumping has also shown higher defect densities in the upper half of the bandgap for HfO$_2$ using the rise and fall time dependence of charge pumping.

A technology that uses molecules to perform the function of electronic components.

C. Richter (NIST)

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• Understanding the electronic structure (energy levels) of molecules is required to develop models of transport.

• In this example, one- and two-photon photoelectron spectroscopy is used to determine the electronic structure around the Fermi level of thiol-bound OPE on Au.

NDR has been observed for many molecules.


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Inelastic tunneling spectroscopy (IETS) can be used to probe molecular vibrational modes and, hence, composition of the SAM.

Inelastic Tunneling Spectroscopy

Spectroscopic characterization of the buried metal-SAM interface can be studied by using infrared radiation through IR-transparent substrates and thin films.

Device = Molecules + Electrodes

*One needs to characterize the molecules with metal gate electrode.

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Within the Device of Interest

**Au (and Al):** minimal perturbation

**Ti:** strong perturbation (but not complete destruction)

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**Backside FTIR**
C. Hacker (NIST)

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Specifications for simply “Replacing the Transistor”
~ $10^{10}$ devices
~ 10 nm feature size
~ $10^{-14}$ sec gate delay
~ 10 year reliability
~ Signal amplification (fan-out)

- There is a fundamental limit to binary logic computing.
- Minimum feature size and switching time for an ideal switch is not too different than a transistor at the end of the roadmap.

![Energy model for limiting device: \( w = \) width of left-hand well (LHW) and right-hand well (RHW); \( a = \) barrier width; \( E_b = \) barrier energy.]

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Emerging Architectures

- Nanocell
- Biologically inspired
- Quantum Computing

Nano-circuit crossbar architecture

Teramac crossbar
• **Biologically inspired architectures** (e.g. the brain) can process large amounts of data in parallel, and are suited to solving ill-defined problems.

<table>
<thead>
<tr>
<th></th>
<th>Binary Limit</th>
<th>Brain</th>
</tr>
</thead>
<tbody>
<tr>
<td># Transistors</td>
<td>~$10^{14}$</td>
<td></td>
</tr>
<tr>
<td># Neurons</td>
<td>~$10^{11}$</td>
<td></td>
</tr>
<tr>
<td># Interconnects/Transistor</td>
<td>~$10$</td>
<td></td>
</tr>
<tr>
<td># Synapses/Neuron</td>
<td>~$10^3$</td>
<td></td>
</tr>
<tr>
<td># Operations/sec</td>
<td>~$10^{12}$</td>
<td></td>
</tr>
<tr>
<td># Operations/sec</td>
<td>~$10^{16}$</td>
<td></td>
</tr>
<tr>
<td>Power Consumption (W)</td>
<td>~$10^6$</td>
<td></td>
</tr>
<tr>
<td>Power Consumption (W)</td>
<td>~$10$</td>
<td></td>
</tr>
<tr>
<td>Reliability</td>
<td>&lt; $1/10^{14}$</td>
<td>Defect Tolerant</td>
</tr>
</tbody>
</table>
Conclusions

• The challenges to metrology for emerging devices and materials are great:
  1. Dimension with Å resolution
  2. Measurements of unknown materials
  3. Composition with atomic resolution
  4. 3-dimensions
  5. Electronic structure and defects at the atomic scale
  6. Measurements within the device of interest

• Device measurements are extremely sensitive to changes in materials and device structure.

• Integrated development of devices, materials, architectures and metrology is crucial.

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